Embedded Non Volatile Memories for Consumer Applications: Status and Perspectives

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• Embedded Non Volatile Memory
  • Challenge and Opportunity
  • Status

• Emerging Technologies
  • Key Features
  • Applications

• ePCRM Overview
Outline

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• ePCM Overview
eNVM Applications

Two key functions
- Code Execution
- Data Management
• Industrial and automotive applications are the most important segments

• MCU market size is expected to grow, as well as the NVM content per MCU

K. Baker, Freescale (IMW 2012)
eNVM Market Challenges

• Market trends impose severe challenges to embedded Non Volatile Memories

• Major factors
  • Price Erosion
  • Fast Program/Erase operation needs
  • Low Power Supply operating conditions
  • High cycling capability
  • Retention
  • Granularity (capability to erase/program Byte or Word)
eNVM Technology Challenges

- Cell Scalability
- Cost
- Performance
- Power Consumption
- Reliability

⚠️ Different ranking of the above parameters depending on the specific application
Today eNVM Solutions

- **EEPROM**
  - Low Power $\rightarrow$ P/E by Fowler Nordheim
  - Reliability
  - Cell Size $\rightarrow$ 2T architecture
  - 15V Operation
  - Bit granularity

- **FLASH NOR**
  - Low Power $\rightarrow$ Programming by Hot Carrier
  - Reliability
  - Cell Size
  - 10V Operation
  - Sector/ page granularity

- **FLASH Split-Gate**
  - Low Power programming $\rightarrow$ SSI
  - Endurance granted by design
  - Cell Size $\rightarrow$ 1.5T
  - Process Complexity
  - Page granularity

- **Low-End products**
  - i.e. mainly driven by cost

- **High-End products**
  - i.e. mainly driven by performances and/or reliability

- **Low Power products**
  - i.e. mainly driven by low power consumption
FG Limiting Factors

- FG cell scalability is achieving its limits
  - Reduced cell current at each techno step → difficult sensing operation between different cell states
  - Reduced coupling factors → increased internal voltage generation to compensate

- FG Program/Erase operations increase internal complexity
  - Flash requires the usage of complex verify algorithm
  - EEPROM requires very high internal voltage to activate the cell
  - Design solution for Low Power Supply embedded products

- Byte or word alterability is still an added value
  - FG is not a universal solution
  - EEPROM or Flash are used according to the application
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Emerging Technologies: the eNVM case

- FG solution is difficult to integrate with high-K metal gate technology for advanced CMOS
- Due to very different applications a single cell/architecture can hardly cover all the needs
- New technologies look-up is essential for the leadership in the eNVM world
Emerging eNVM

- **Key factors**
  - Easy to integrate into the baseline logic platform
  - Suitable to fit application requirements
  - Cost

- **Guidelines**
  - Integration in the Back-End of the process (after contact definition)
    - Compact cell area
    - No impact on CMOS
  - Reliability and Low Power
    - Wide range of applications
    - Automotive (Zero Defect requirements) should rely on volume production, possibly for Stand-Alone memories (same as today FLASH route)
  - Few additional masks
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From MRAM to STRAM (1/2)

**MRAM**
- Assessment of field MRAM for High Reliability applications (16Mb, 1.42μm² cell size at 180nm node, IBM 2004)
- Need read before write
- Poor scalability below 90nm

**STRAM**
- Perpendicular Magnetic Anisotropy (PMA) materials mandatory for low write current
- $\Delta R/R \sim 200\%$ to be compatible with CMOS ➔ very low reading window available for memory industry
- Trade-off between low write current density and thermal stability
- STRAM technology is challenging (very complex multi-layer stack)
From MRAM to STRAM (2/2)

MRAM BUILDING BLOCK: THE MTJ

- Nevertheless there is an increasing interest from industry…
RRAM (1/2)

• The Resistance change is due to formation and dissolution of a conductive filament in a dielectric layer

• Three categories
  1. Unipolar systems (thermally assisted, very high current)
  2. Bipolar Conductive Bridge (CBRAM): electrochemical dissolution and re-deposition of an active electrode
  3. O-RRAM: based on movements of Oxygen anions

R.Waser, IEDM 2011 Tutorial

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RRAM represents one of the most interesting technology solutions for alternative eNVM - especially for Low Power applications.

Nevertheless, storage mechanism is not fully understood.

Reliability assessment of RRAM technology is far from maturity level reached on PCM:
  - Long-term reliability (solid extrapolation at 10y)
  - Retention vs write power
  - Trade-off between cycling and HTDR
  - Behavior at very high temperature (>100C)

Some hints but no data on scalability.
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New Materials: Past and Future

Semiconductor industry has been driven by introduction of new materials over decades
Chalcogenide Alloys over Decades

- Reference Phase Change material for memories is $\text{Ge}_2\text{Sb}_2\text{Te}_5$
ePCM Competitive Advantage

- Easier to be integrated with advanced logic
  - lower voltage
  - no impact on CMOS front-end

- Cost-effective
  - few additional masks (only 3 masks overhead for storage element definition)
  - smaller cell vs. EEPROM, smaller over-head vs. FLASH

- Better performance
  - single bit over-write
  - programming speed
  - endurance
A true 3D integration of Non Volatile Memory
ePCM Outlook

• PCM is the most mature among novel memory concepts
  • Micron and Samsung starting stand-alone memory production at 45nm

• Embedded PCM Technology is developed in synergy with stand-alone mainstream
  • Same storage element, with MOS as selector
  • Feasibility at 90nm node demonstrated for consumer applications

• Embedded PCM can be a real breakthrough for process cost saving and performances
  • NVM integrated in BEOL
  • Best in class for power consumption and write data throughput, perfectly fitting contact-less secure microcontrollers requirements
High level of confidence in terms of:

- **Yield**
  - \( \sim 90\% \) on 4Mbit Test Chip (with redundancy)

- **Reliability**
  - 10y retention at 85C granted
  - \( >10M \) cycles cell level
  - 1ppm defectivity after 100k cycles: solid data collection on 4Mb

- **Storage Mechanism**
  - Retention vs write power
  - Failure modes
• Less critical than FLASH memory in terms of
  • Cycling at High Temperature
  • Retention after cycling
  • Extended endurance

• New retention concept
  • It is a matter of probability for crystallization
  • No “weak” bits in the array
e-PCM integration – 4Mbit Test Chip

- A 4Mbit Test Chip integrated in 6 metal levels 90nm process for extrinsic evaluation of e-PCM cell
Set and Reset Distributions

• A strong cell-level signal (3 decades change in resistance) must be translated in reading window in the µA region

Read Window
25µA

Ref. Current
16µA

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ePCM for Low Power

- Thanks to
  - Medium Voltage operation (<3.3V)
  - Very fast Reset operation (<100ns)
  - Low current Set operation (~I_{reset}/2)
  - Low Voltage Read operation (<1.2V)
  - GO1 Row/Column decoder
  - Bit alterability (no need of Erase before Program)

- ePCM solution results best-in-class in terms of
  - Electrical performances (access time, consumption, throughput)
  - Capability to achieve aggressive contact-less requirements
- ePCM Cell is defined by:
  - Circuitry rules in Y direction
  - Reset current in X direction

- Aggressive cell area in the range of 18F² can be obtained
  - Still room for improvement with proper GST optimization, e.g. by doping
  - Cell scalability granted for next technology nodes (65nm, 45nm and beyond)

- Very compact macrocell results from small circuitry overhead needed for row/column decoder, charge pumps, no recovery algorithms
Commonly used Ge$_2$Sb$_2$Te$_5$ has crystallization temperature close to 150C:
- No way to preserve code content after soldering (2min at 260C)
- Big challenge and refresh concept to fit automotive specs (some years HTDR at 150C)

By modifying the percentage of Ge-Sb-Te in the alloy, crystallization temperature ranging from 150C up to 400C have been obtained

Customization of material inside ternary diagram is feasible (i.e. retention, SET speed or programming current)
Conclusions (1/2)

• MCU market size is expected to grow, as well as the NVM content per MCU, so representing an important business opportunity

• By considering scaling trends, FG solution seems difficult to integrate with high-K metal gate technology for advanced CMOS

• Among emerging technologies, the whole family of RRAM and the STRAM appear particularly appealing (in particular, CBRAM seems promising for Low Power applications)

• Nevertheless, it is a long journey towards a reliable industrial solution…
Conclusions (2/2)

- PCM is the most mature among novel memory concepts (production started at ~Gb densities and ~45nm technology node)
- Embedded PCM Technology is developed in synergy with stand-alone mainstream and can be a real breakthrough for process cost saving and performances
- Major progress in Materials Exploration activity
  - 10 years HTDR at T>150C demonstrated cell level
  - Good confidence to overcome soldering limitations
  - Key features for Low Power applications confirmed
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