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spintec SPIN IN ELECTRONICS

Hybrid CMOS/Magnetic integrated electronics

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Workshop on Innovative Memory Technologies
2012, June 21 - MINATEC, Grenoble - France

Grenoble INP | UNIVERSITE JOSEPH FOURIER SCIENCES. TECHNOLOGIE. SANTÉ | cnrs | cea

OUTLINE

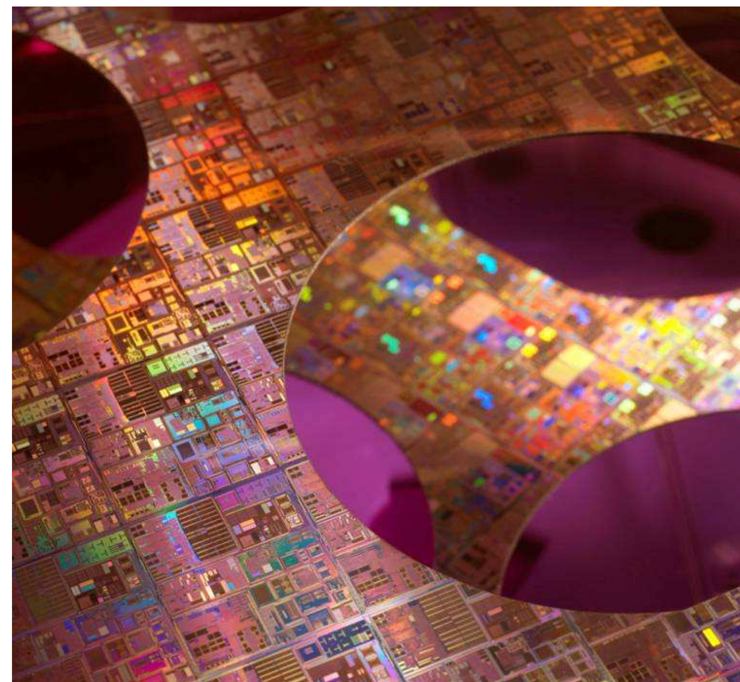
Basic phenomena used in spintronic devices
Tunnel MR, Spin-Transfer Torque (STT)

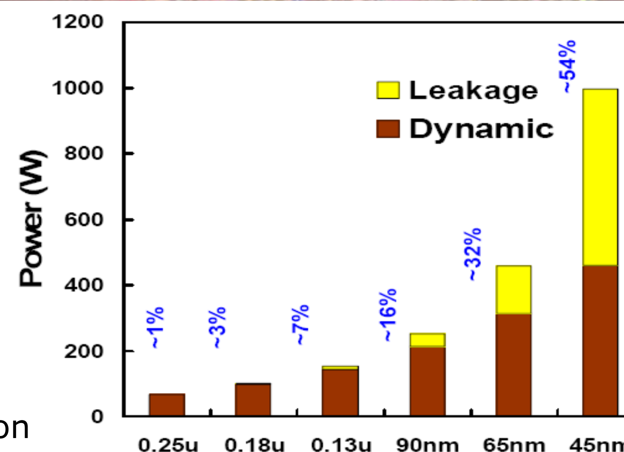
Various categories of MRAM

MRAM written by Spin Transfer Torque (STT MRAM)
Downsize scalability below 20nm

Extended scalability and new functionalities of MRAM using thermally assisted writing

Low-power and reconfigurable electronics based on hybrid CMOS/MTJ technology





Transistor scaling will result in higher leakage currents for volatile memory and logic gates.
Energy savings by combining non-volatile memory and logic functions.

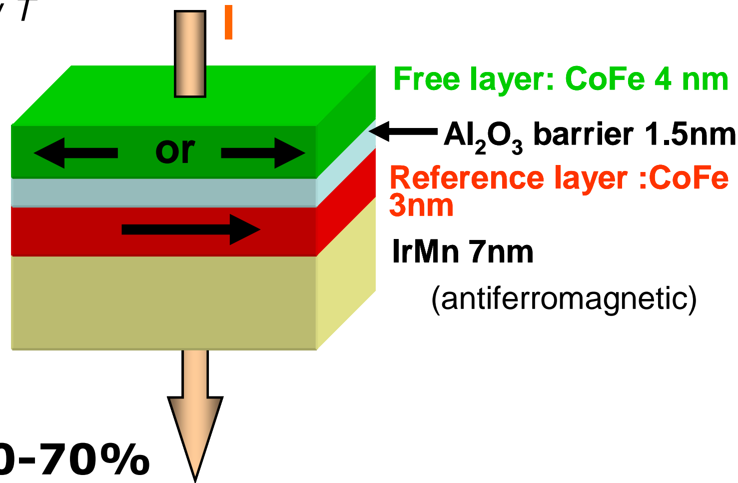
Non-Volatile Logic:
Combining non-volatile elements to reduce standby power consumption

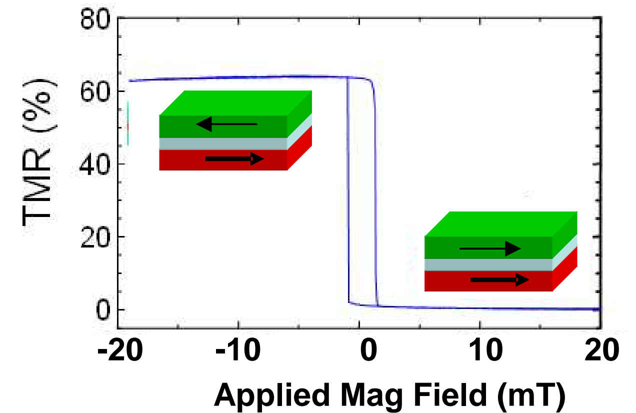
Tunnel Magnetoresistance (TMR)

Tunnel magnetoresistance at RT in magnetic tunnel junctions (MTJ):

Julliere (1975) but only at low T
Moodera et al, PRL (1995);
Myazaki et al, JMMM(1995).

Like couple polarizer/analyzer in optics





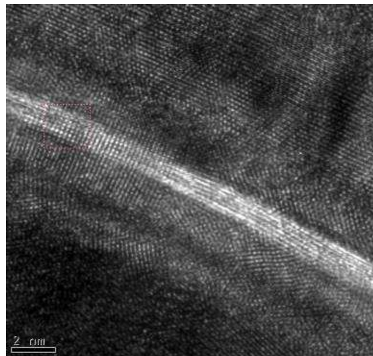
$TMR=(R_{AP}-R_P)/R_P \sim$ **40-70%**

Giant tunnel magnetoresistance in crystalline MgO based MTJ

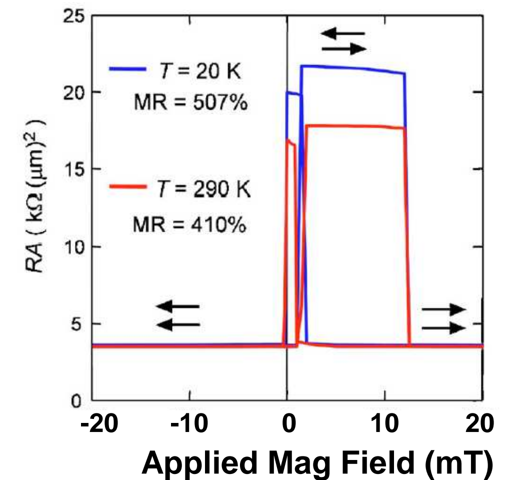
Parkin et al, Nature Mat. (2004);
Yuasa et al, Nature Mat. (2004).

TMR~ **100-600%**

Crystalline:
Additional spin-filtering mechanism according to symmetry of electron wave functions



Au cap 50 nm
Ir-Mn 10 nm
Fe(001) 10 nm
Co(001) 0.57 nm
MgO(001) 2.2 nm
Co(001) 0.57 nm
Fe(001) 100 nm
MgO(001) 20 nm
MgO(001) sub.

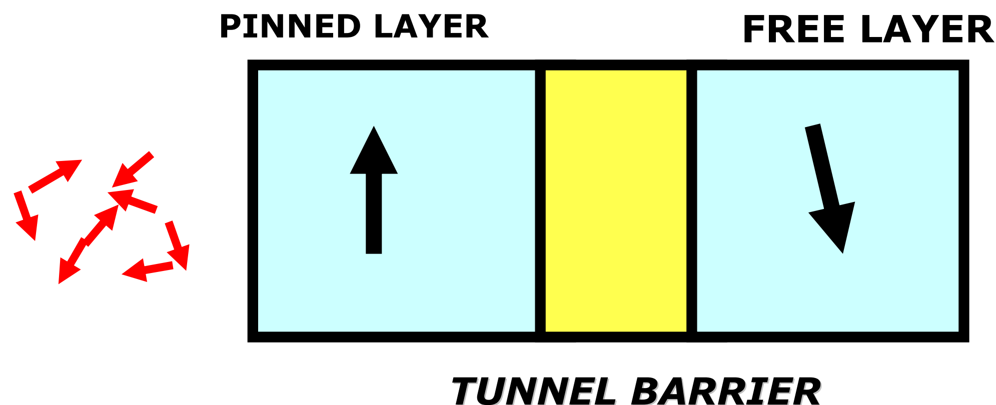


Spin-Transfer Torque (STT)

Predicted by Slonczewski (JMMM.159, L1(1996)) and Berger (Phys.Rev.B54, 9359 (1996))

Giant or Tunnel magnetoresistance:
Acting on electrical current via the magnetization orientation

Spin transfer is the reciprocal effect:
Acting on the magnetization via the spin polarized current



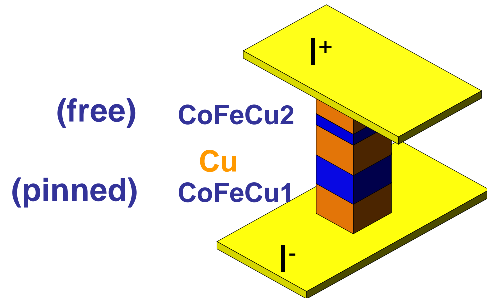
M.D.Stiles et al, Phys.Rev.B.66, 014407 (2002)

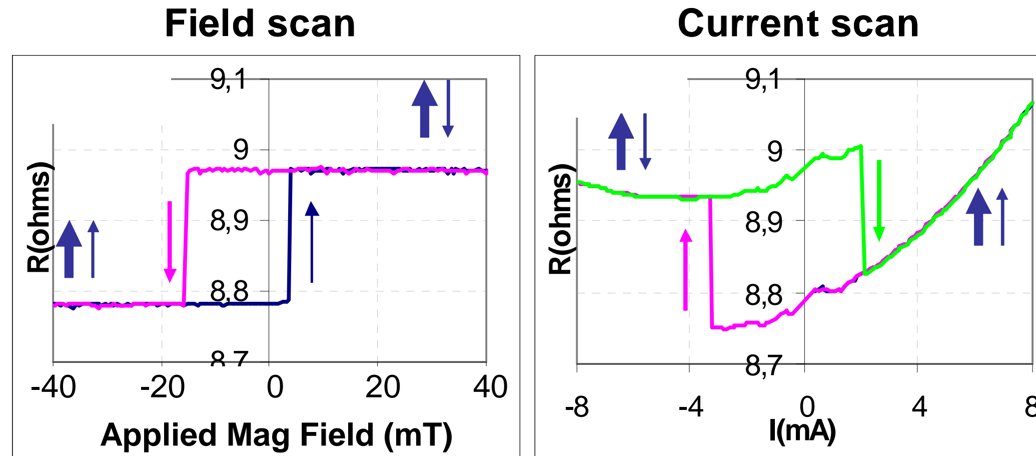
Reorientation of spin polarization ⇒**Torque on the free layer magnetization**

A new way to manipulate the magnetization of magnetic nanostructures

STT induced magnetization switching

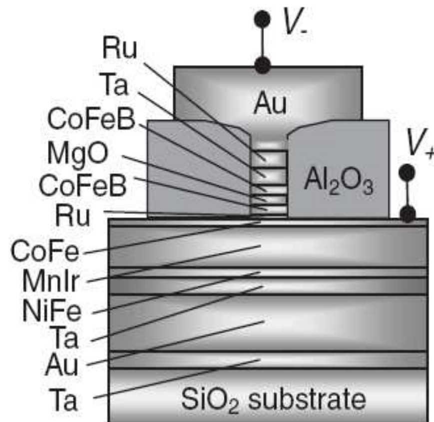
First observation in fully metallic structures (Co/Cu/Co sandwiches Jc ~2-4.10^7A/cm²)
Katine et al, Phys.Rev.Lett.84, 3149 (2000)



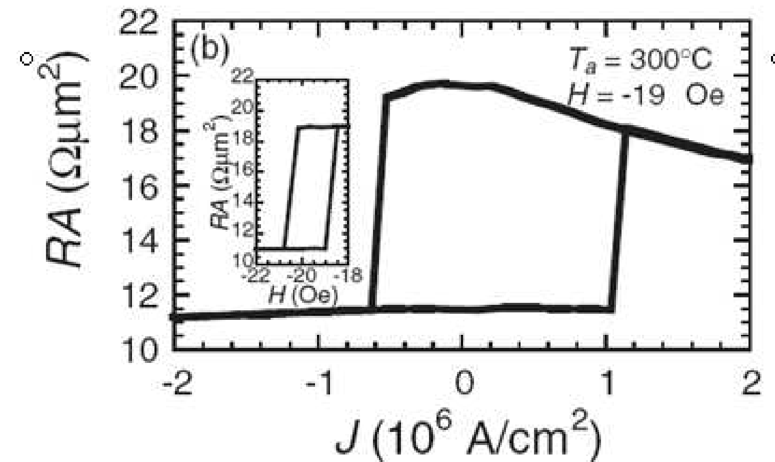


Deac A, Lee KJ, Liu Y, et al.Phys.Rev.B73 (6), 064414 (2006)

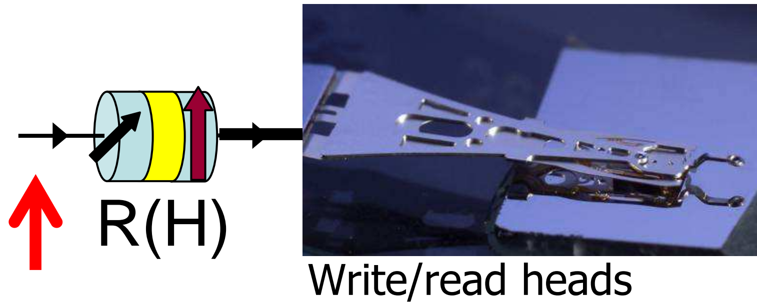
First observation in MTJ : Huai et al, APL (2004); Fuchs et al, APL (2004) (Jc ~10^6A/cm²)



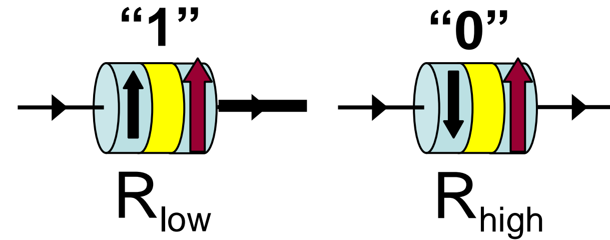
Hayakawa et al, Japanese Journal of Applied Physics 44, (2005),L 1267



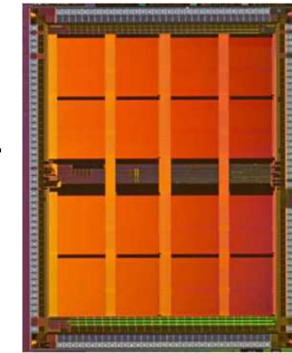
Spintronic components



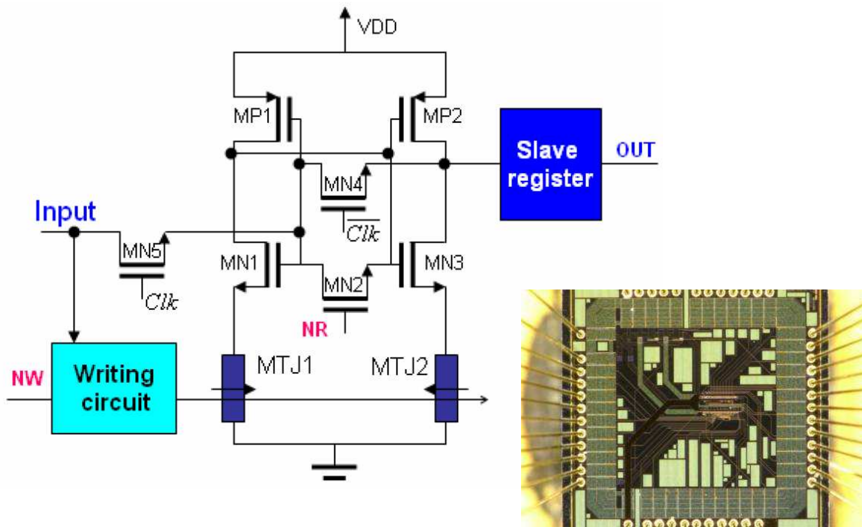
Magnetic field sensors



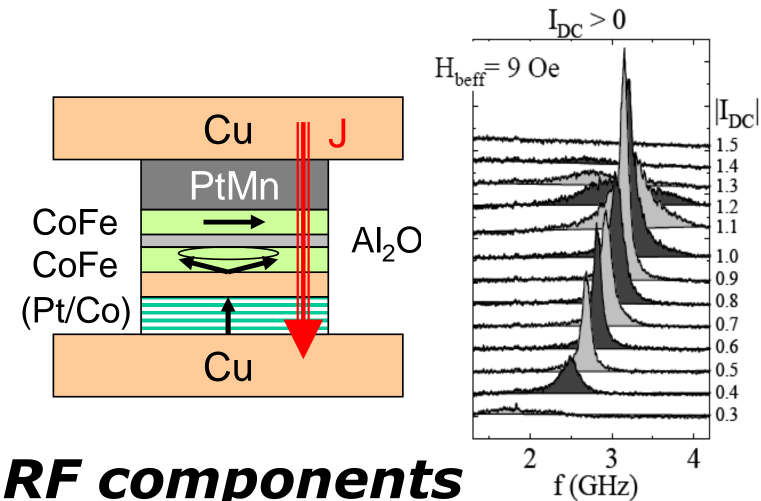
Memories



Everspin 4Mbit



Logic circuits

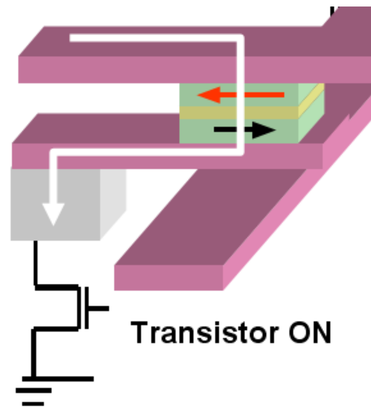


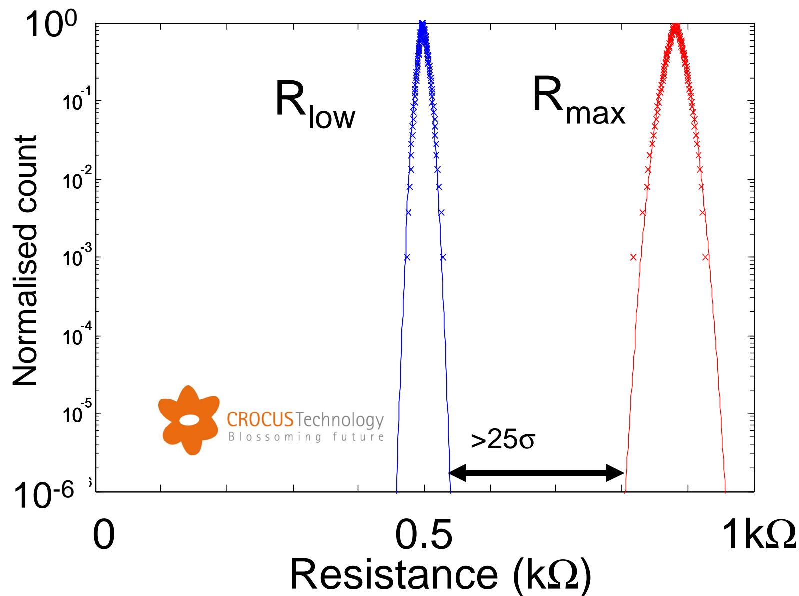
RF components

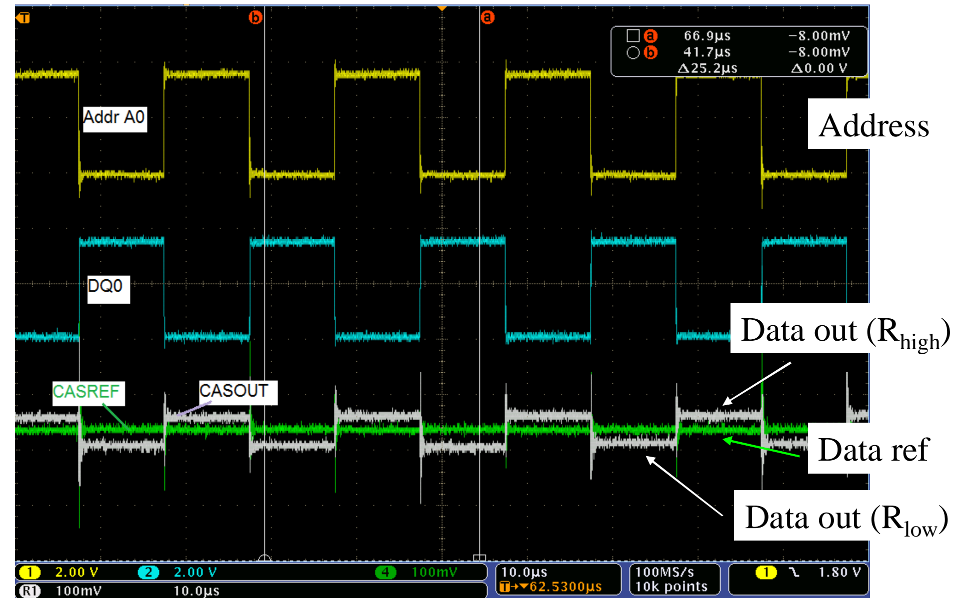
Dieny B et al, Intern.Journ.Nanotechnology, 7, 591 (2010).

MRAM basics - Read

Read data by sensing the cell resistance and comparing to a reference cell

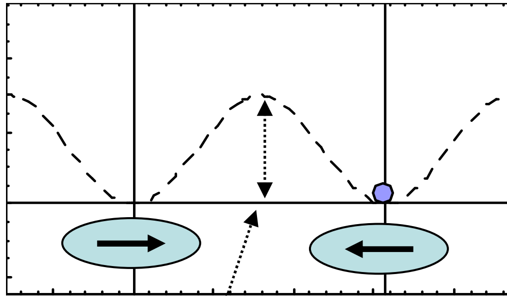






Read @ 20ns in products
Down to sub-10ns demonstrated

MRAM basics - Store


Stability barrier K_uV

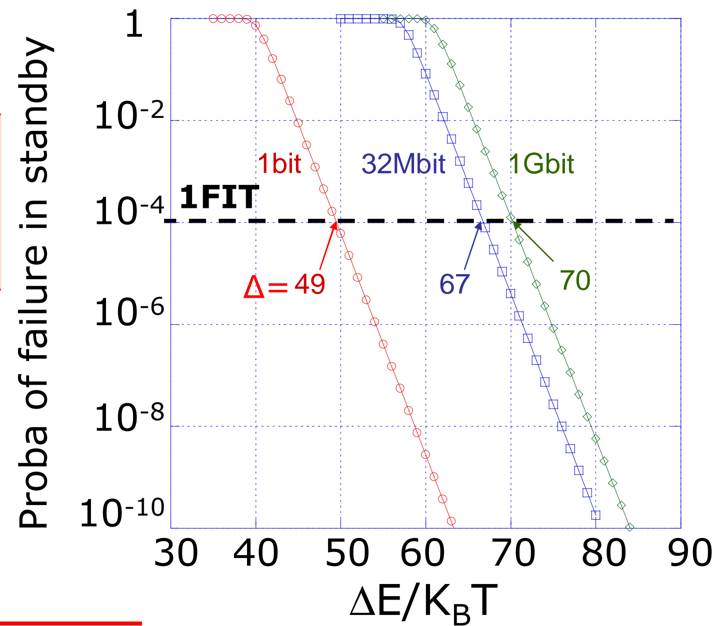
Switching rate $\tau = \tau_0 e^{\frac{\Delta E}{k_B T}}$

- K_uV
- ΔE ← *Barrier to overcome for switching*
- $k_B T$ ← *Thermal activation*
- $t_0 = 10^{-9}$s

Switching probability for one bit $P_{\pm} = 1 - e^{-\frac{t}{\tau_{\pm}}}$

Probability of Accidental switching for N bits: $F(t) = 1 - \exp(-Nt/\tau) = 1 - \exp\left[\frac{-Nt}{\tau_0}\exp\left(-\frac{\Delta E}{k_B T}\right)\right]$

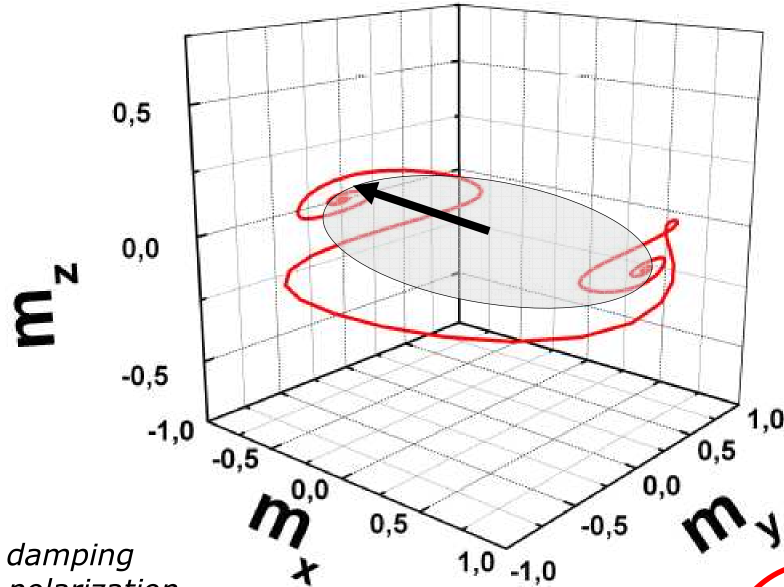
For 1 bit, 10 years retention → $\Delta E/k_BT > 49$
For 1 Mbit, → $\Delta E/k_BT > 67$
For 1 Gbit → $\Delta E/k_BT > 70$



Key role of the thermal stability factor
$\Delta = \Delta E/k_B T$

In-plane versus out-of-plane STT switching

In-plane magnetized MTJ



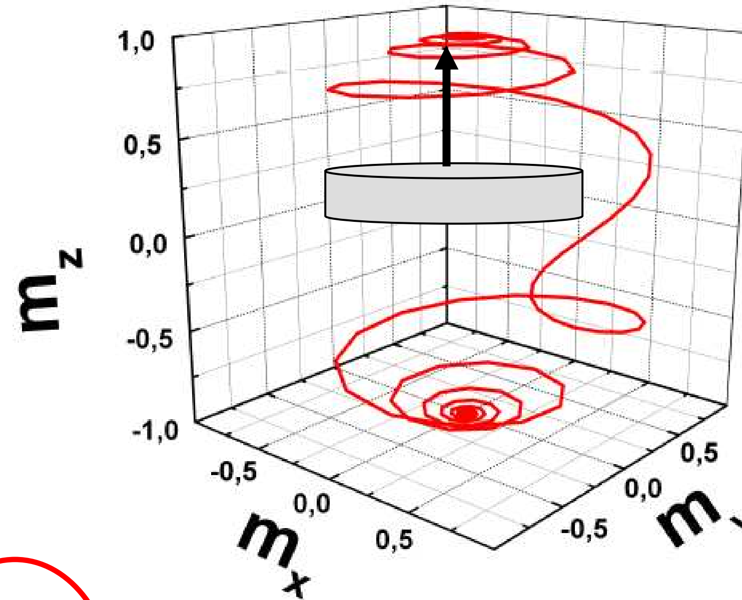
α = damping
p = polarization
A = Area
g(0)~1

$$j_c^{in-plane} = \left(\frac{4e}{\hbar}\right)\frac{\alpha k_B T}{g(0)pA}\left(\Delta + \frac{\pi M_s^2 V}{k_B T}\right)$$

Thermal stability determined by in-plane anisotropy (shape anisotropy)

Simpler materials but additional penalty in jc due to out-of plane precession

Out-of-plane magnetized MTJ

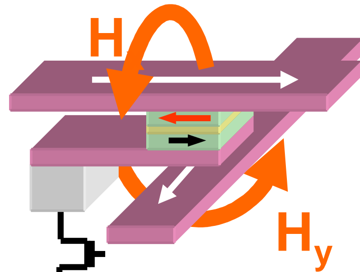


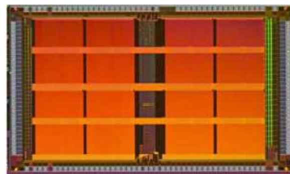
$$j_c^{perp} = \left(\frac{4e}{\hbar}\right)\frac{\alpha k_B T}{g(0)pA}\Delta$$

More complex materials but lower jc expected thanks to direct proportionality between Jc and thermal stability

Various MRAM differing by their write principle

Field-only « Toggle »





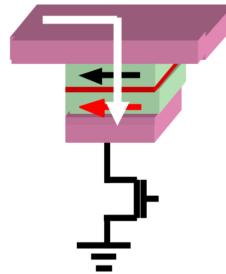
1, 4, 16Mb Toggle (2006)

Established technology
1.5M units shipped
4.5M forecasted in 2011

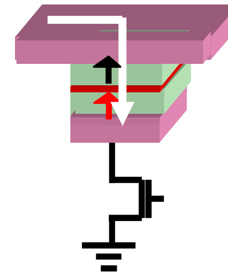
Not scalable beyond 90 nm

Spin Transfer Torque « STT » or « SPRAM »

Planar



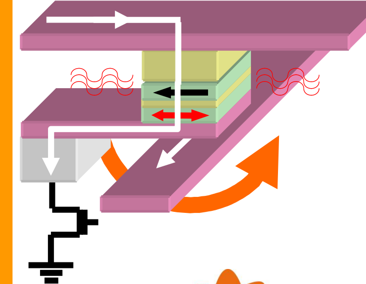
Perpendicular



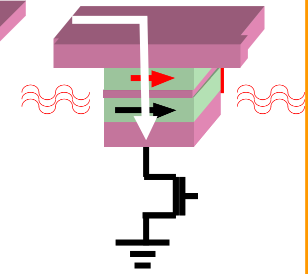
Lower write current
Minimal cell / array size
Scalable down to 14nm with dual p-MTJ

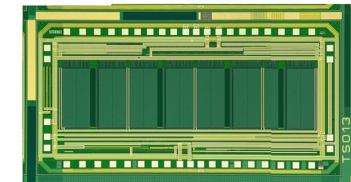
Thermal Assist « TAS » or « TAMRAM »

Field-TAS



STT-TAS

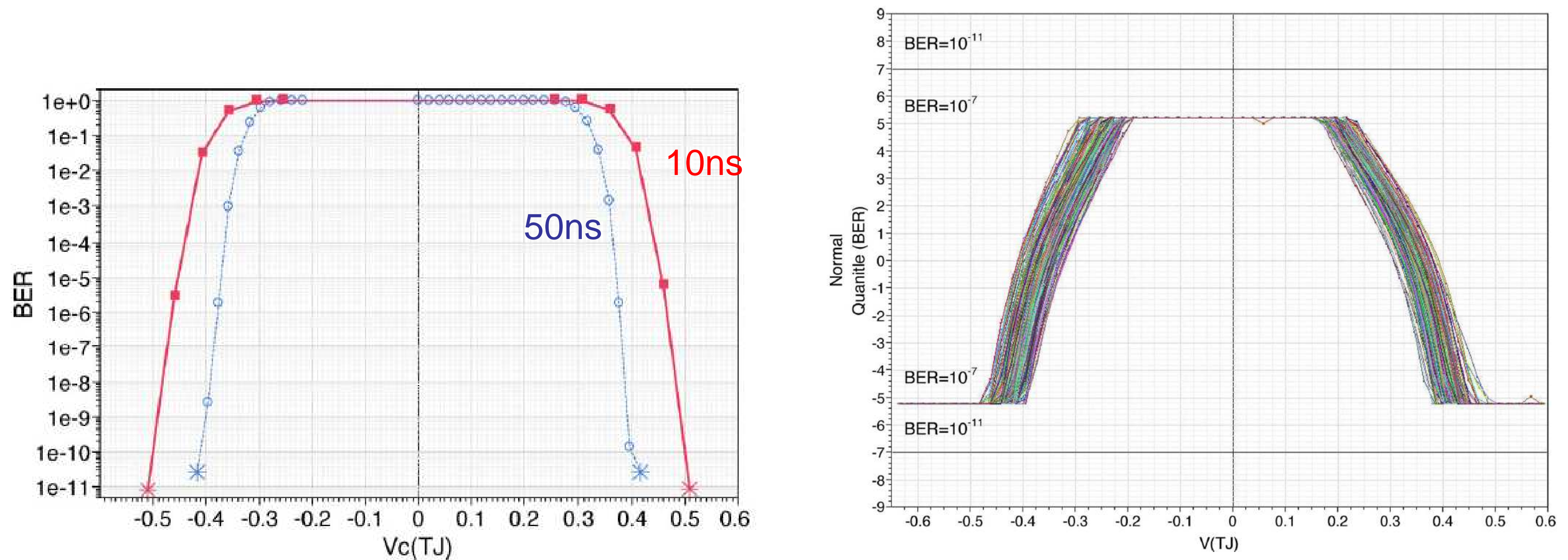




Crocus 1Mb Field-TAS (2011)

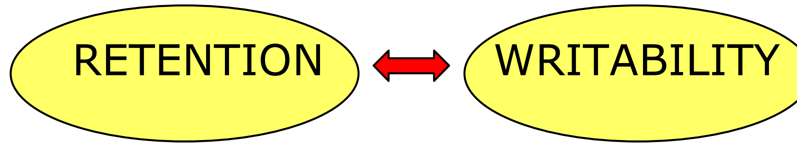
Scalable down to ~ 10nm
High stability
Multibit possible

Recent Perpendicular STT Demo Chips



Thermally Assisted writing (TA)

Purpose: Solve the dilemma between

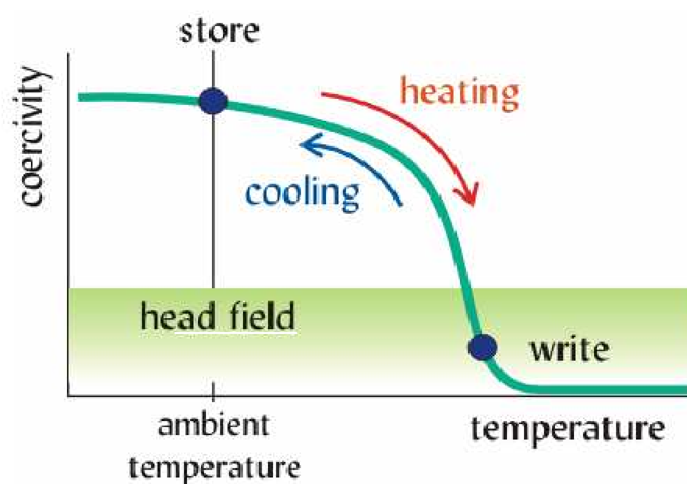


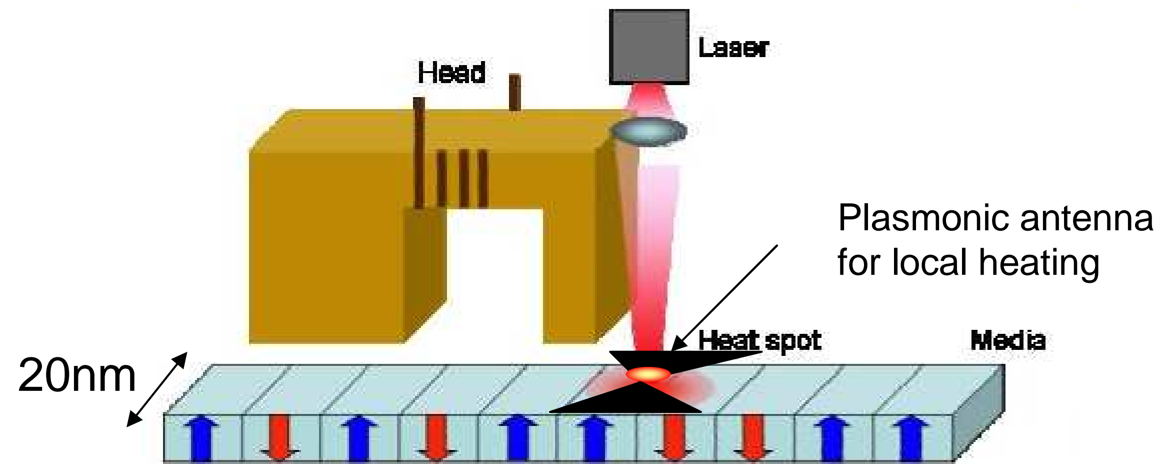
e.g. $I_{write}^{perp} = \left(\frac{4e}{\hbar}\right)\frac{\alpha}{g(0)P}k_B T.\Delta$

•Use temperature-dependence of switching ability

- **Write at elevated temperature**
- **Store / read at room temperature**

•Same basic concept as in **Heat Assisted Magnetic Recording** in hard disk drive technology

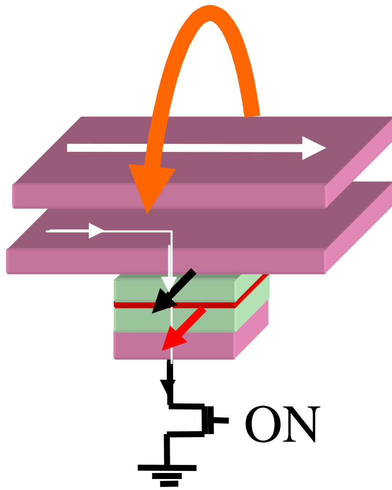


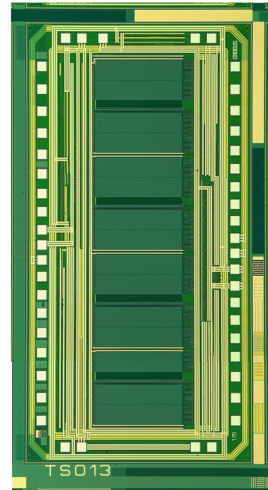


B.C.Stipe et al, Nature Photonics 4, 484 (2010)

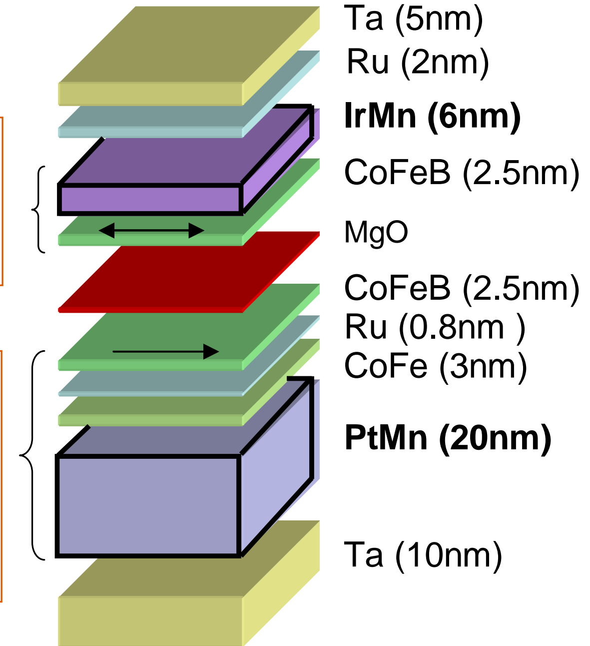
- **In MTJ for MRAM, heating produced by Joule dissipation around the tunnel barrier**.
- Write temperature~250°C

Thermally Assisted MRAM written by Field

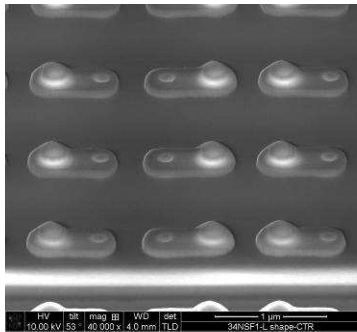




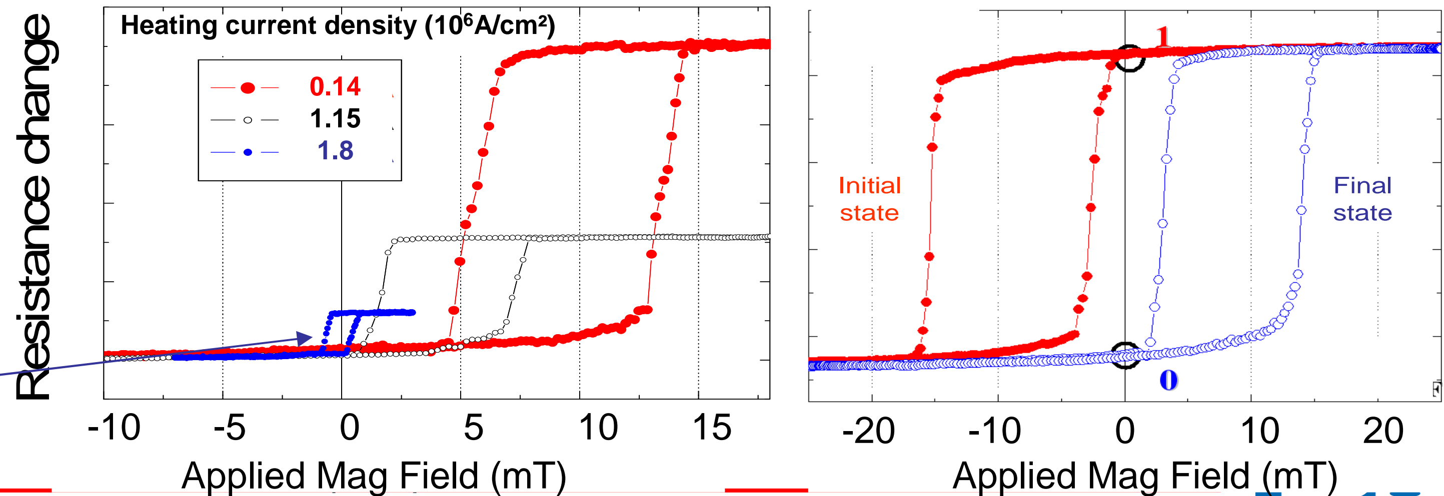
1 Mbit chip



Dieny B et al, Intern.Journ.Nanotechnology, 7, 591 (2010).



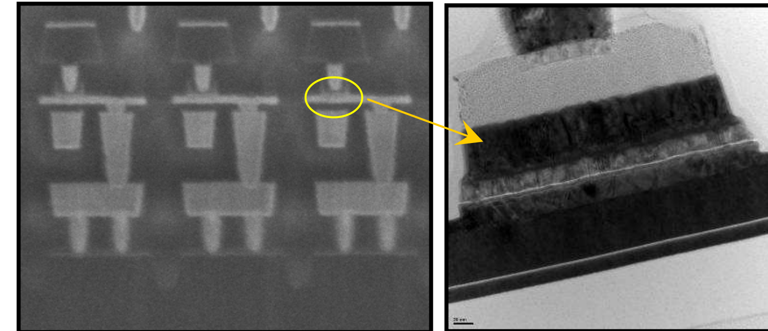
Low switching field at write temperature thanks to circular bit shape

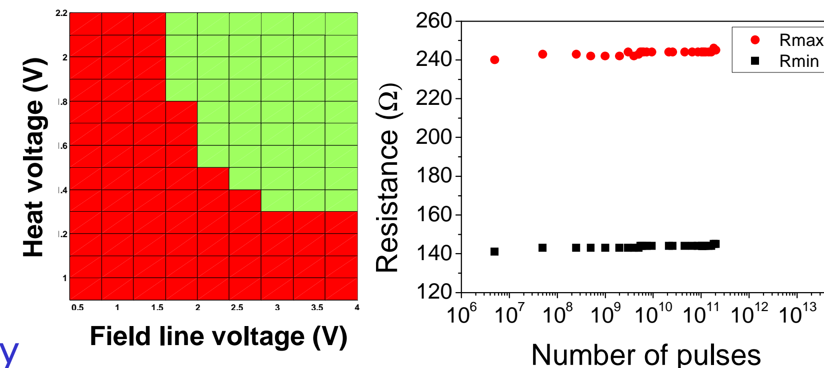


Thermally Assisted MRAM written by Field

1Mbit chip SRAM compatible demonstrator
130nm technology

- Writing demonstrated down to 10ns pulses (*thermal rise time ~5ns)*
- Write voltage level controlled through engineering of thermal barriers
- Write field of 2mT can be used instead of 7mT in toggle MRAM (thanks to circular pillar)
- External field immunity on stored data verified up to 15mT





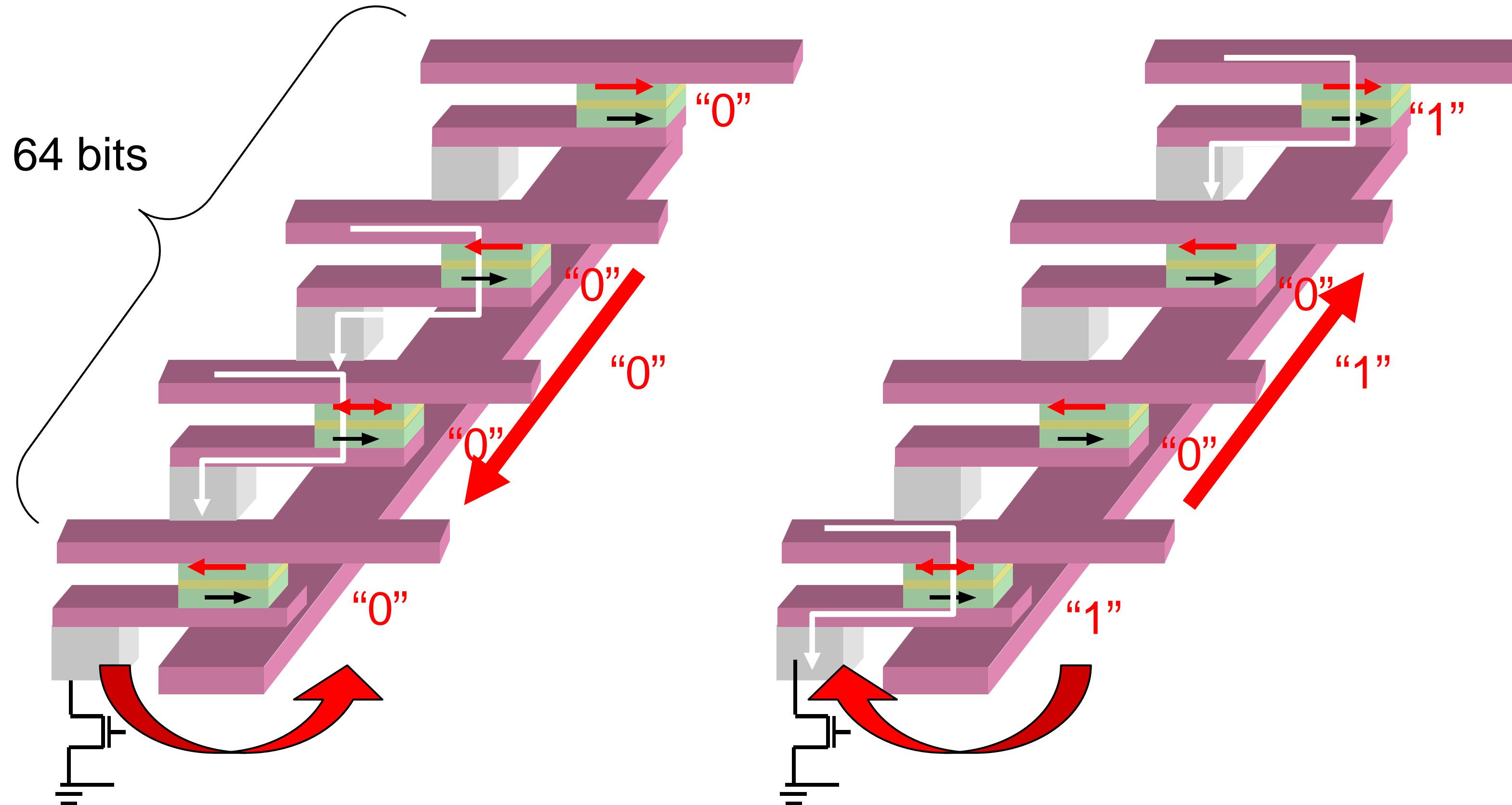
Low write field thanks to circular shape MTJ.
Thermal stability not provided by a shape anisotropy but by pinning of the storage layer at RT

With $K_{IrMn}=3.10^6 erg/cm^3$,

$D=KV/K_BT>200$ for 50nm diameter
$D=KV/K_BT=70$ for 12nm diameter

Very good downsize scalability provided by Thermal Assistance

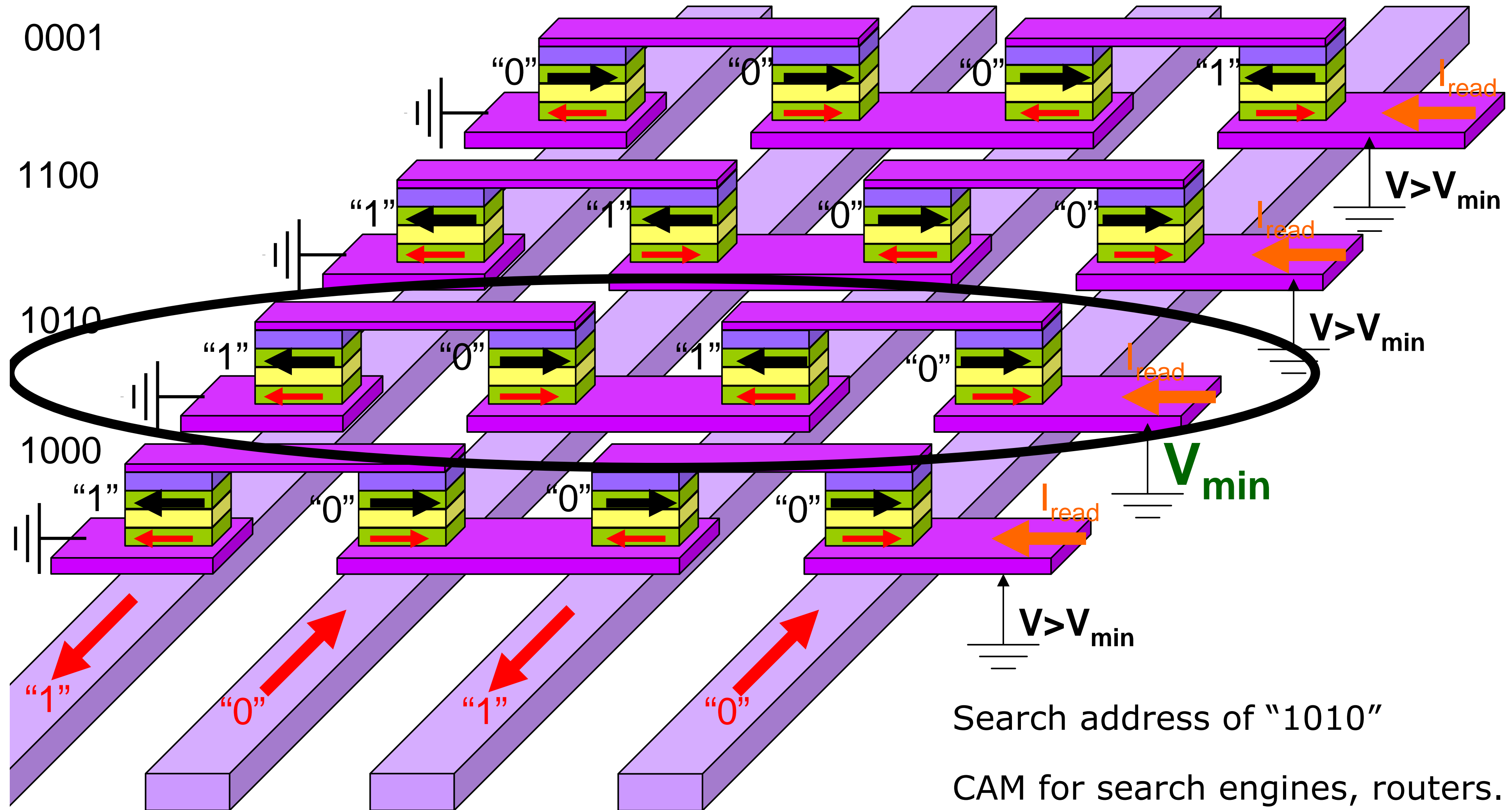
Write sequence (Field-TA-MRAM)



Only 2 pulses of field required to write 64bits vs 65 pulses in toggle.
Required field ~ 3-5mT vs 7-10mT in toggle

Energy per 10ns field pulse over 64bits=35pJ i.e. 0.55pJ per bit
Energy per 10ns heating pulse = 1pJ per bit, similar to STT writing

TA-MRAM as Content Addressable Memory (CAM)



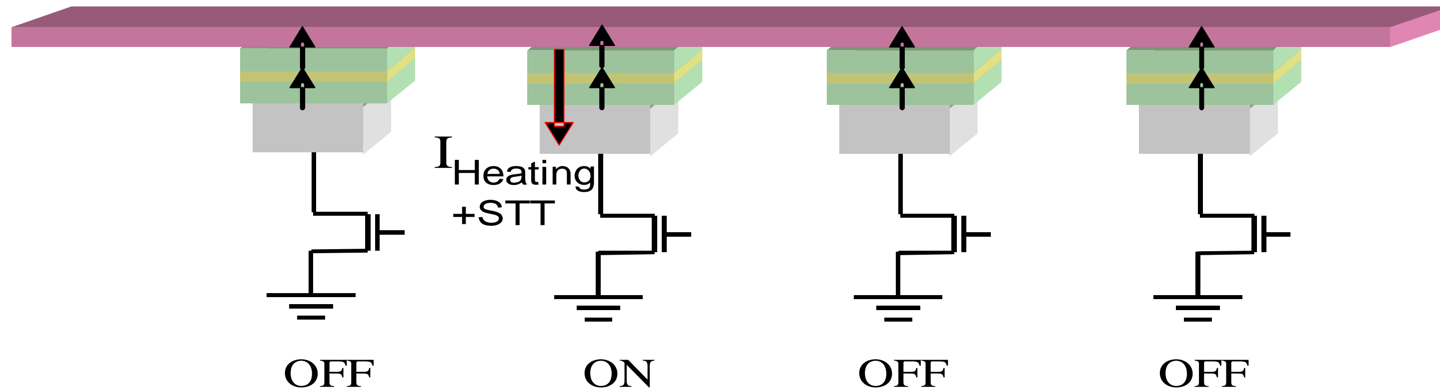
Search address of "1010"

CAM for search engines, routers.

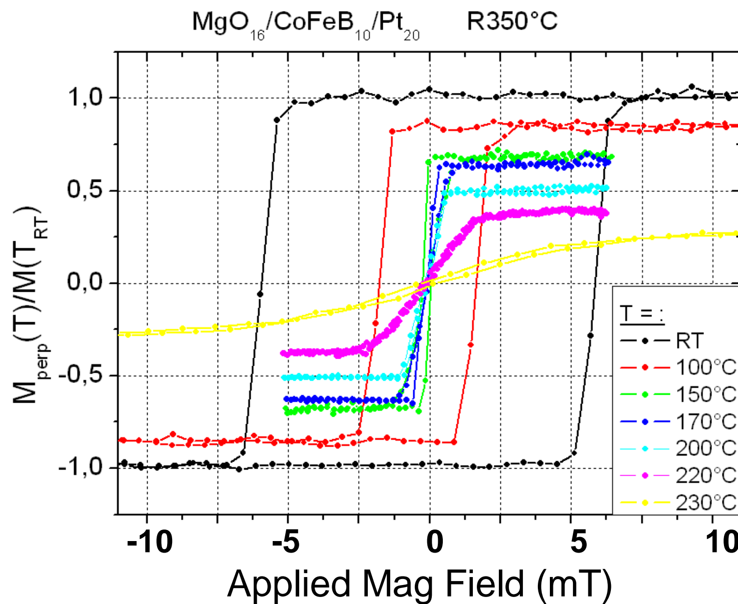
Intrinsically combines memory and XOR functions: **Magnetic Logic Unit (MLU)**
"**Match-in-Place**" ⇒ security applications

Thermal assistance in perpendicular STT-MRAM

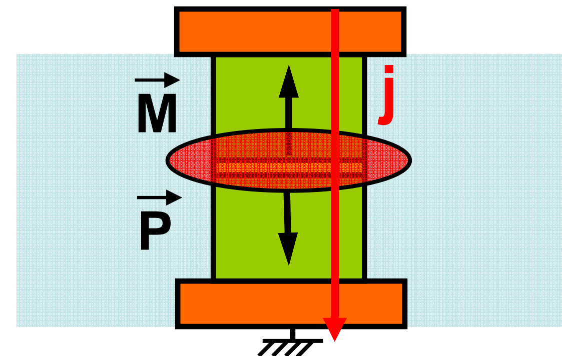
TAS + STT



Takes advantage of a thermally induced anisotropy reorientation



S.Bandiera et al, APL 2011



$$\vec{M} \perp \vec{P}$$

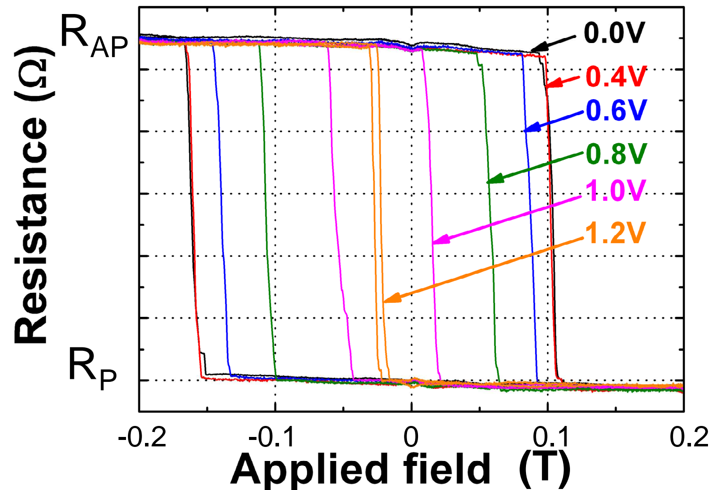
$\vec{M} \wedge \vec{P}$ **max**

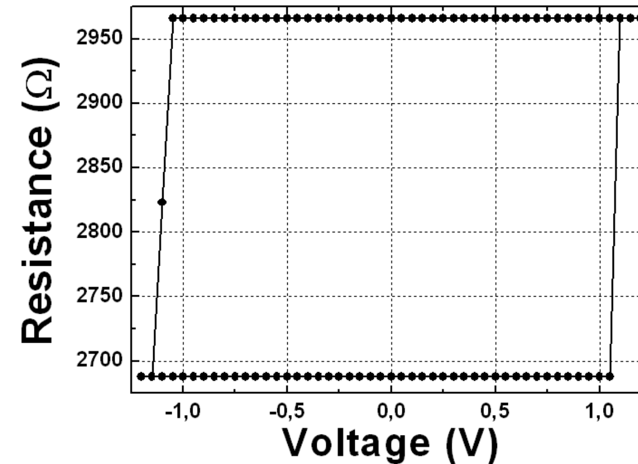
$\vec{T}_{STT}$ **max**

Max STT efficiency

Thermal assistance in perpendicular STT-MRAM

p-MTJ with (Pd/Co)/CoFeB/MgO/CoFeB/(Pd/Co)





S.Bandiera et al, APL 2011

Very significant decrease in coercivity versus bias voltage due to Joule heating around the tunnel barrier

Figure of merit:

$$\frac{\Delta}{I_c} = \left(\frac{4e}{\hbar} \frac{\alpha}{P} k_B T \right)^{-1}$$

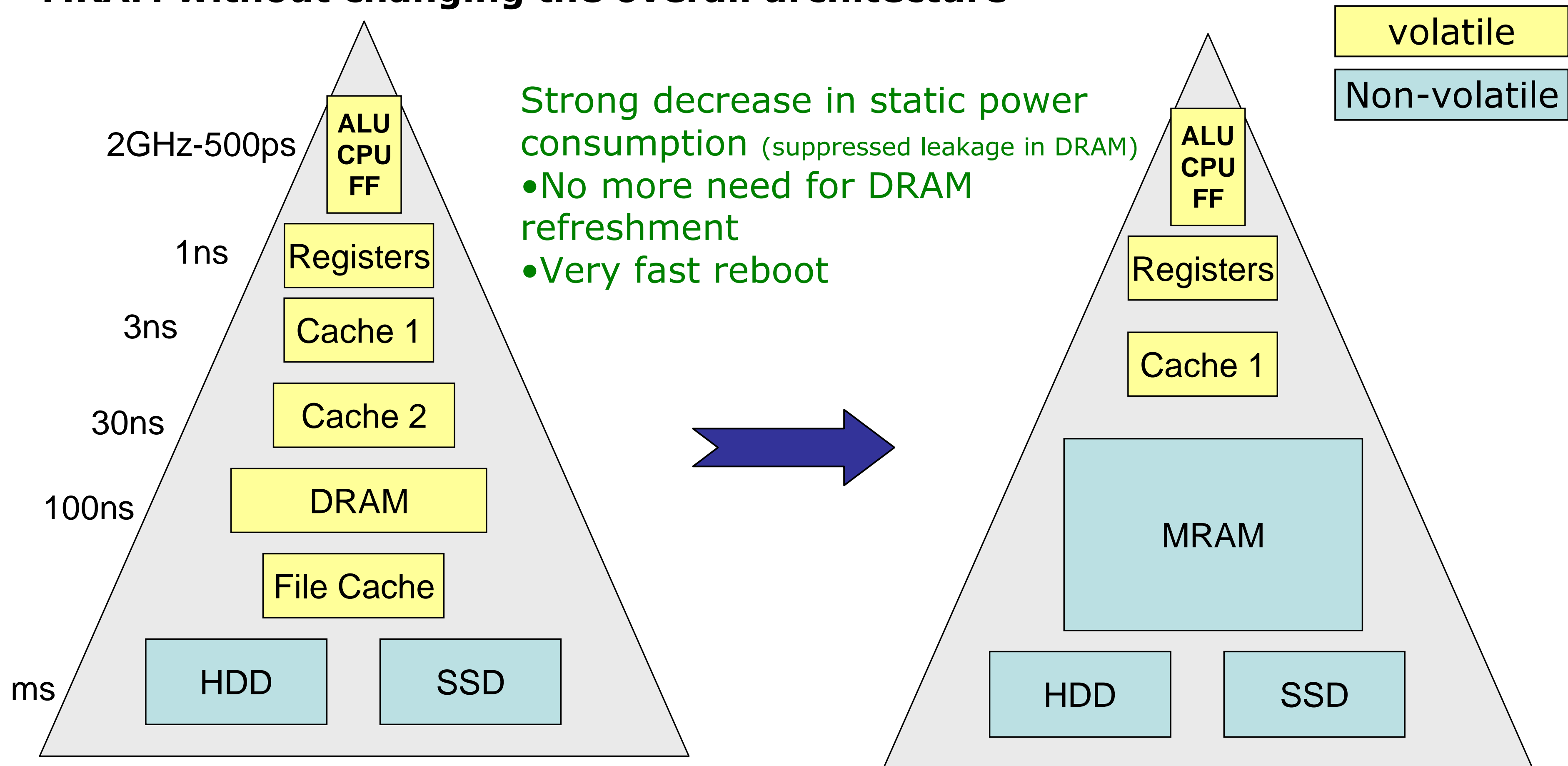
Figure of merit

Reference	Material	J_c(30ns) (MA/cm²)	Δ(d=40nm)	Δ/I_c	TMR(%)	α
Nakayama et al. (2008)	CoFeB/ TbFeCo	4,9	10	2	10	?
Ohno et al. (2010)	CoFeB/ MgO	3,8	43	113	120	0,013
Worledge et al. (2011)	CoFeB/ MgO	2,8	20	71	46	0,04
This work (2011)	CoFeB/ (Pd/Co)	4,6	73	159	10	0,15

Largest Figure of Merit ever reported thanks to TA+STT

Where MRAM can help ?

1) In memory hierarchy, replacement of DRAM or Cache 3 or 2 by STT MRAM without changing the overall architecture



(Samsung, Hynix/Toshiba: replacement of DRAM by STT-MRAM beyond the 20nm node)

T.Kawahara, IEEE Design and test of computers, 52, Janv/Feb 2011)

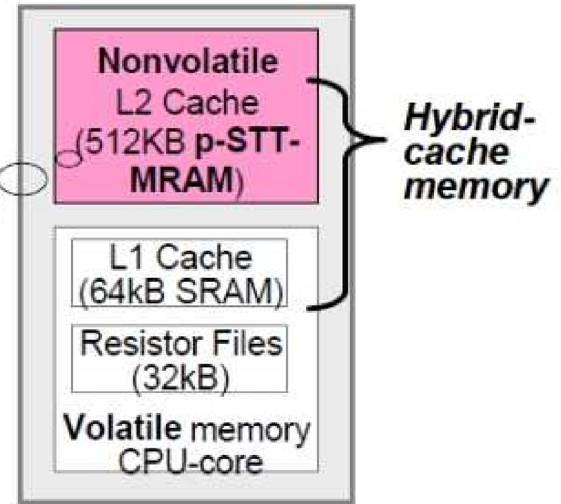
Normally-OFF Computers

Toshiba Proposes MRAM/SRAM Hybrid Cache for Normally-off Computers

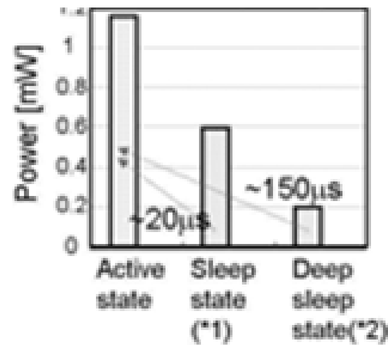
Nov 8, 2011 18:39
Motoyuki Oishi, Nikkei Electronics

L1 cache : Volatile memory (SRAM)
L2 cache : Non-volatile memory

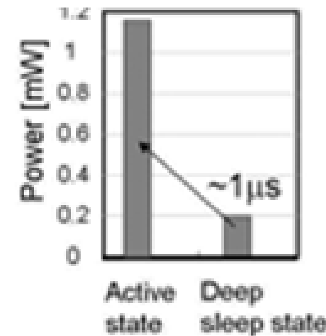
Low Static Power.
Fast wake up from power gating mode....



Conventional power gating



Ultrafast power gating

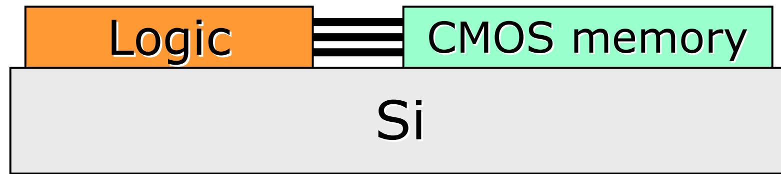


2) Tighter integration between logic and memory

Dieny B et al, Intern.Journ.Nanotechnology, 7, 591 (2010).

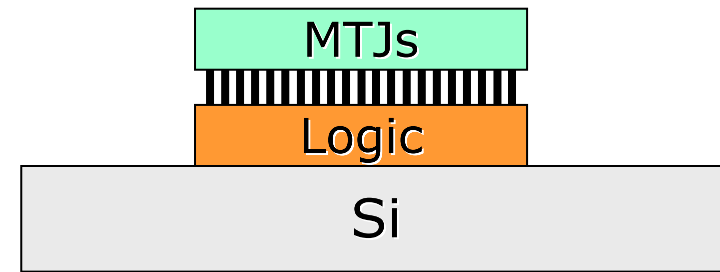
Same technology as for MRAM

With CMOS technology only:



-Slow communication between logic and memory
-few long interconnections
-Large capacitive dynamic losses
-complexity of interconnecting paths
-large footprint on wafer

With hybrid CMOS/magnetic:
"Logic-in memory"

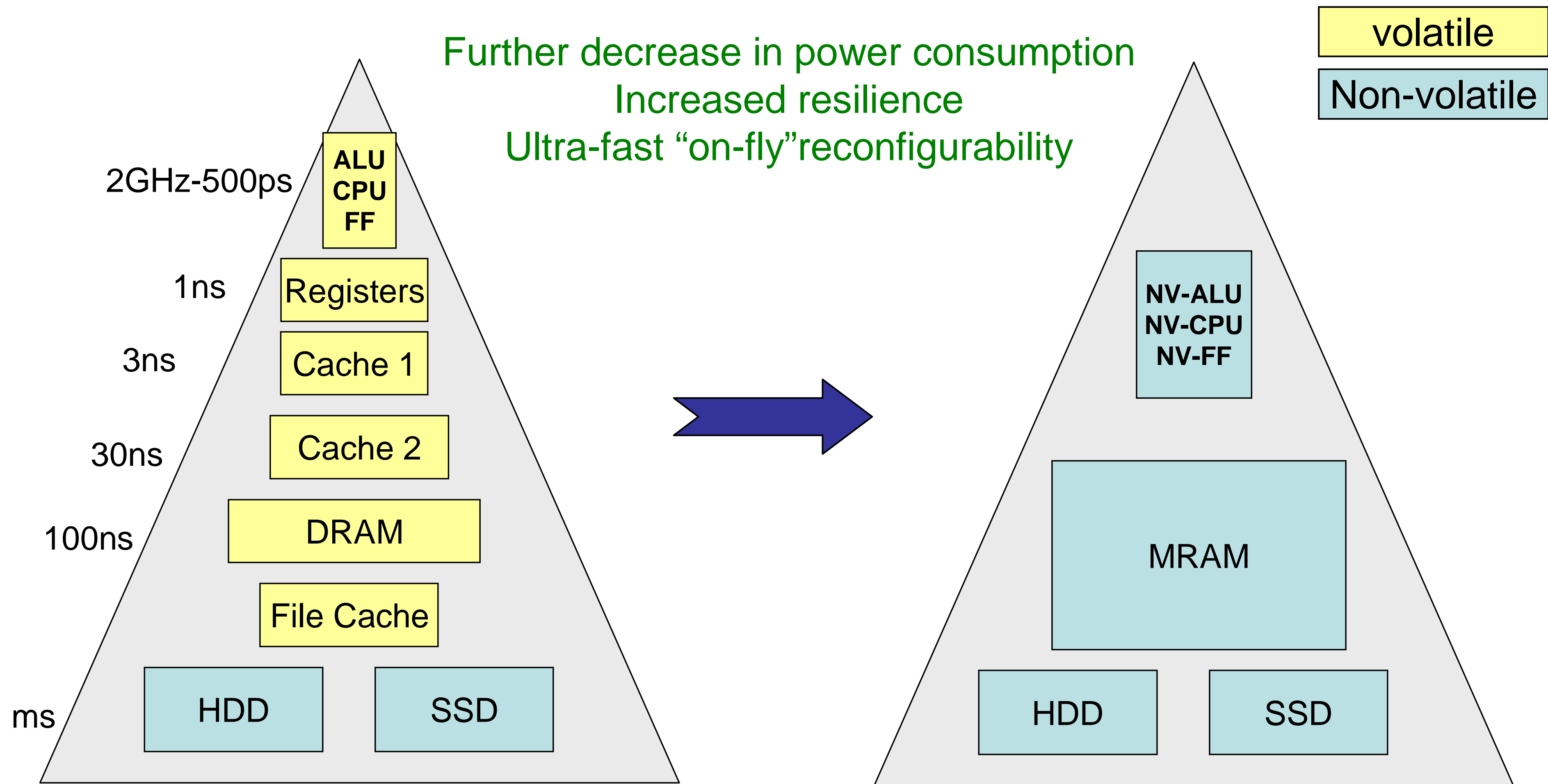


-Memory much closer to logic
-Large static and dynamic energy saving ("normally-off / Instant-on computing")
-Fast communication between logic and memory
-Numerous short vias
-Simpler interconnection paths
-Smaller footprint on wafer

New paradigm for architecture of complex electronic circuit (microprocessors..)

Where MRAM can help ?

3) With ultrafast MRAM (~300ps), non-volatily can be introduced in the logic gates (Flip-flop, ALU…)



T.Kawahara, IEEE Design and test of computers, 52, Janv/Feb 2011)

Magnetic non-volatile logic circuits

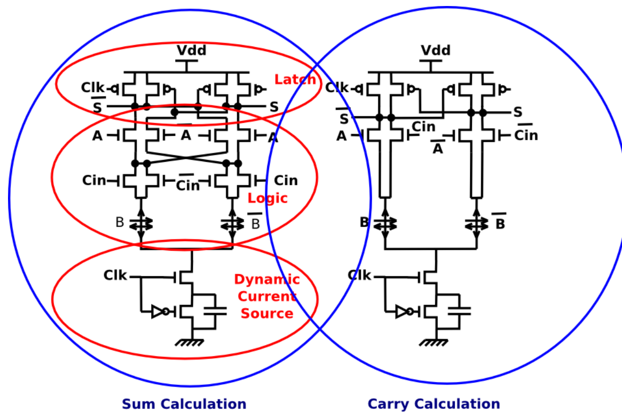
Hitachi + Tohoku University

S.Matsunaga et al, Applied Physics Express, vol. 1, 2008.

Non volatile Full Adder

One input is made non-volatile (instant startup, security)

– Demonstrator : CMOS 0.18µm,



	CMOS	Hybrid CMOS/Mag
Delay	224 ps	219 ps
Dynamic Power	71.1 µW	16.3 µW
Writing Time	2 ns/bit	10 (2) ns/bit
Writing Energy	4 pJ/bit	20.9 (6.8) pJ/bit
Standby Power	0,9 nW	0 nW
Surface	333 µm²	315 µm²

Reduced power consumption

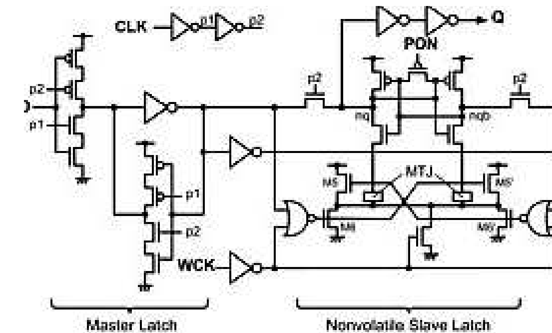
Reduced footprint

See also Y.Gang et al, IEEE Trans.Mag.47, 4611 (2011)

NEC Empowered by Innovation

Home > News Room > NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs

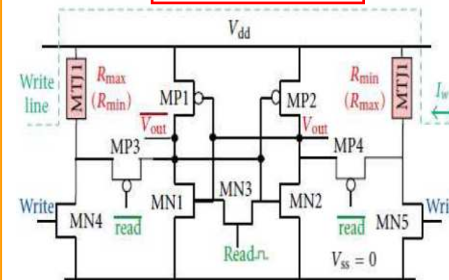
NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs



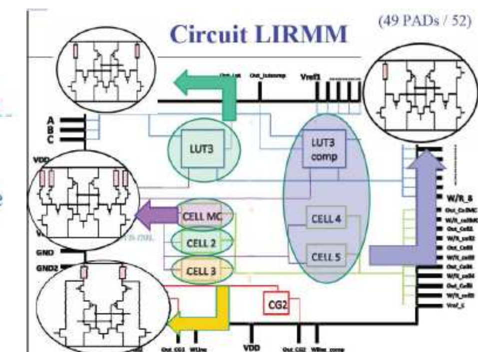
spintec SPIN IN ELECTRONICS

LIRMM

NV-SRAM



Magnetic LUT



Conclusion

•Purpose of hybrid CMOS/Magnetic technology is to combine the best of the two worlds

CMOS	**Magnetism**
Speed, low dynamic power consumption perfect for logic	*Non-volatility of magnetization perfect for memory*

•Increasing interest for p-STT MRAM for standalone, embedded memories or logic-in-memory. Scalability down to 14nm with dual p-MTJ.

•Thermally assisted writing allows to extend the downsize scalability, reduce power consumption and introduce new functionalities in MRAM (e.g. Match-in-Place)

•Manufacturing technology getting more and more mature with a growing number of actors

•Huge potential development

Acknowledgements

B.Dieny
R.Sousa
J.Herault
S.Bandiera
Y.Hadj-Larbi
B.Rodmacq
S.Auffret
M.Souza
L.Nistor
JP Nozieres

L.Buda-Prejbeanu
J.C.Toussaint
I.Firastrau
M.Chsiev
B.Belhadji
H.Bea
S.Amara
V.Baltz
J.Moritz

I.L.Prejbeanu
K.Mackay
L.Lombard
E.Gapihan
C.Ducruet
Y.Conraux
C.Portemont
J.Shin
K.Azizpor
D.Beery
Y.Cohen
J.Reid
B.Cambou

O.Redon
B.Delaet
M.T.Delaye
M.C.Cyrille

Work partly supported by the projects

RAMAC (ANR 2007)

CILOMAG (ANR 2007)

NANOINNOV SPIN (2009)

HYMAGINE (ERC2009)

PATHOS (ANR 2010)

Thank you !