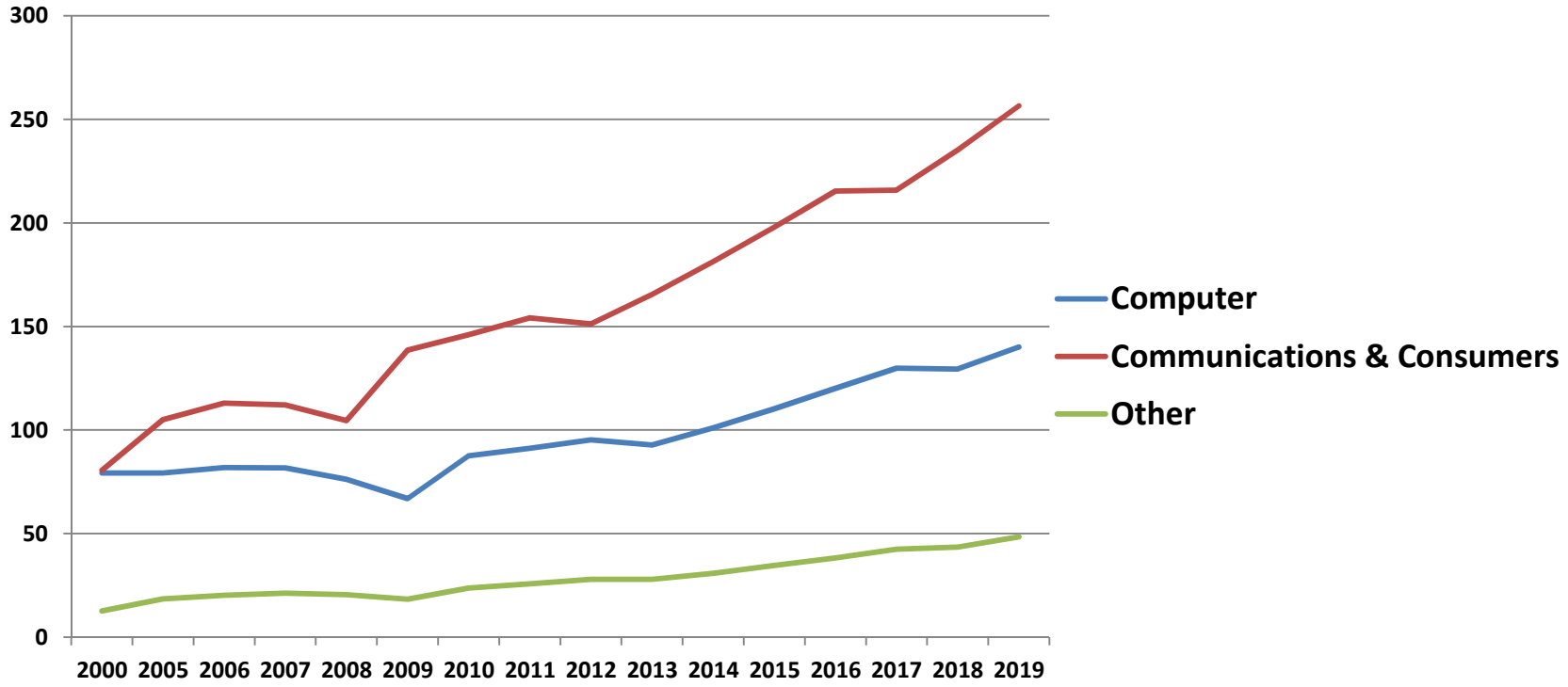
Using OxRAM for saving power in FPGA architecture: what can we expect?

Fabien Clermidy

IC market trends: Applications

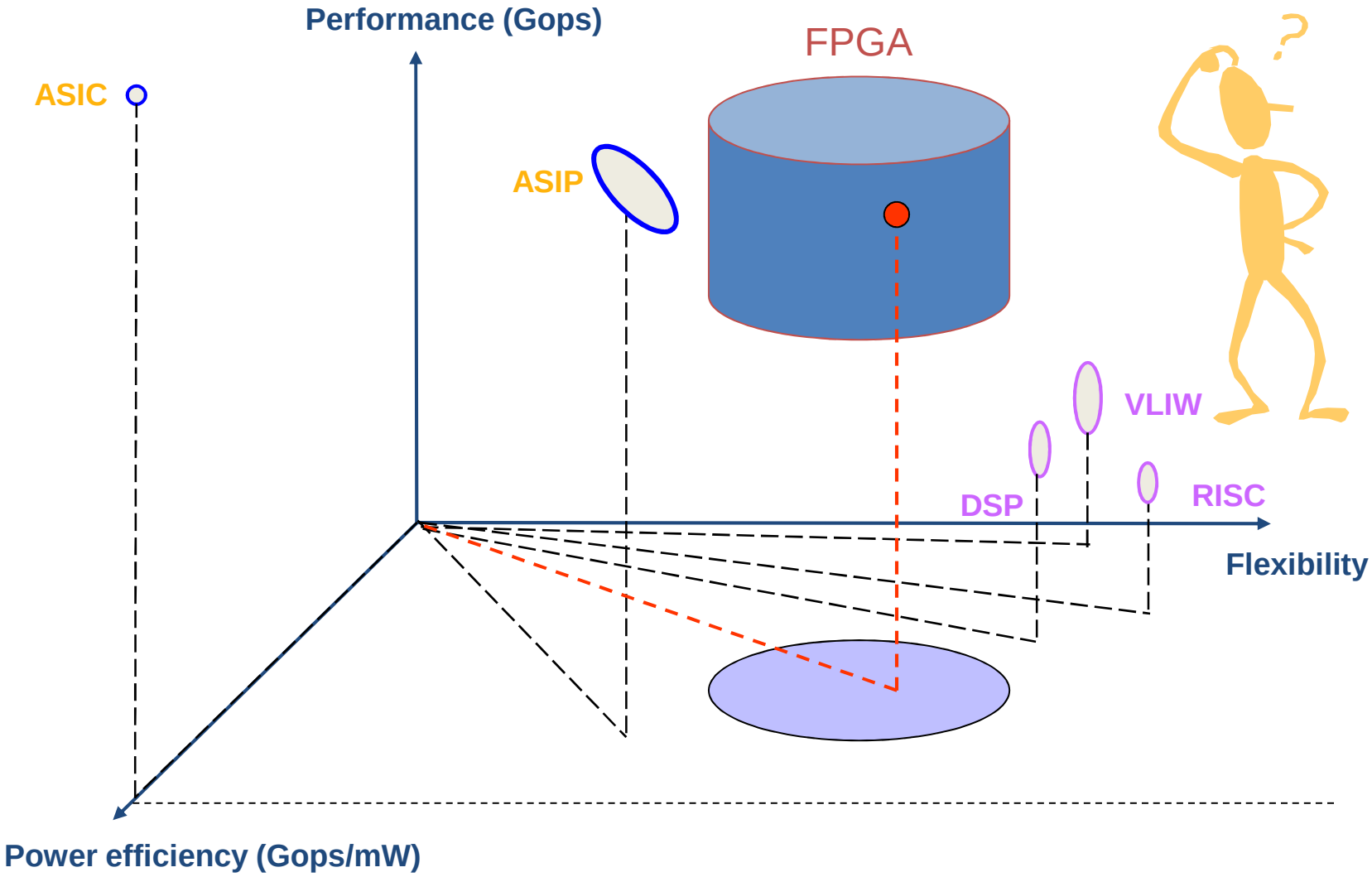
- Communications and consumers products outperform computers since 2000
- New applications appear => autonomous systems



What is an autonomous system?

- Pervasive electronic not visible from final user
- Sleep mode is the normal mode
- Wake-up must be fast, high computing demand in burst mode
- Multiple applications but low to medium market size for each application
- Examples:
  - Smartgrids
  - Health-care systems
  - Sensor Networks

Architecture for autonomous systems?



FPGA Market

- About 90% of market controlled by SRAM-based FPGA
  - Long set-up time
  - Large power consumption

Low Price
Or
high Capacity

- Non-volatile FPGA opportunities
  - Instant power up
  - Data integrity
  - low power modes

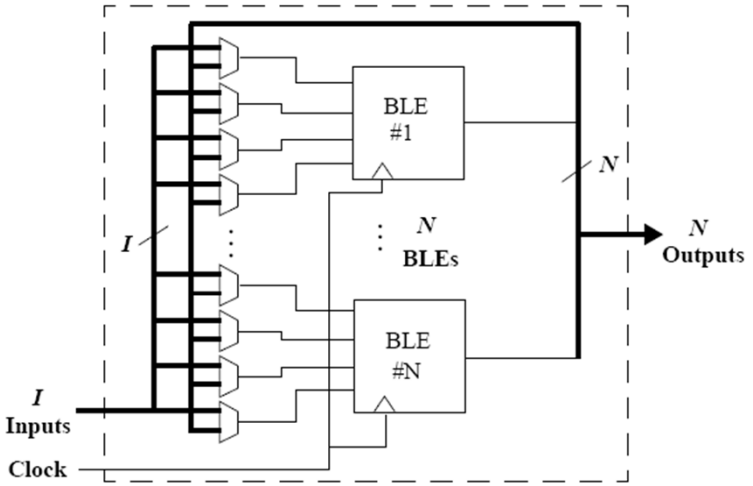
High Price
Low Capacity

→ Small niche applications : Space, Defense

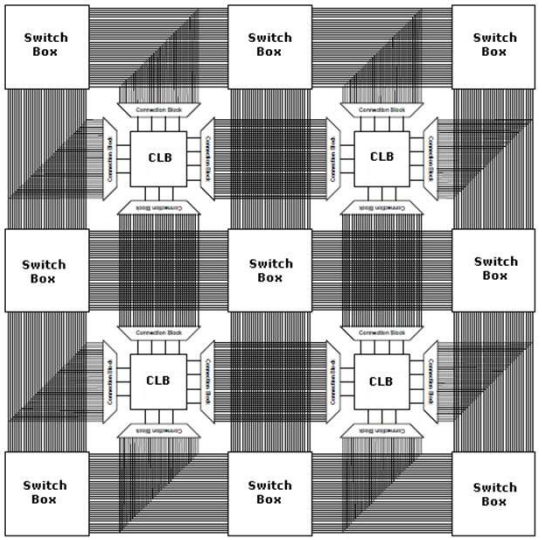
FPGA for autonomous systems

- ✓ Flexible / adaptable
- ✓ Scalable
- ✓ High performance
- ✓ Simple and fast boot procedure (no software stack)
- ✓ Dynamic power consumption
- ✓ High leakage

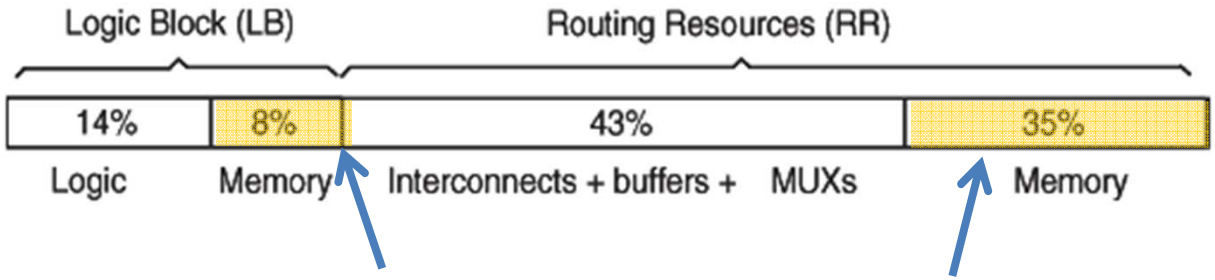
Field Programmable Gate Array



Ahmed et al., 2001



Logic element = CLB



Lin et al., 2007

Mainly configuration memories

Instantly-on operation

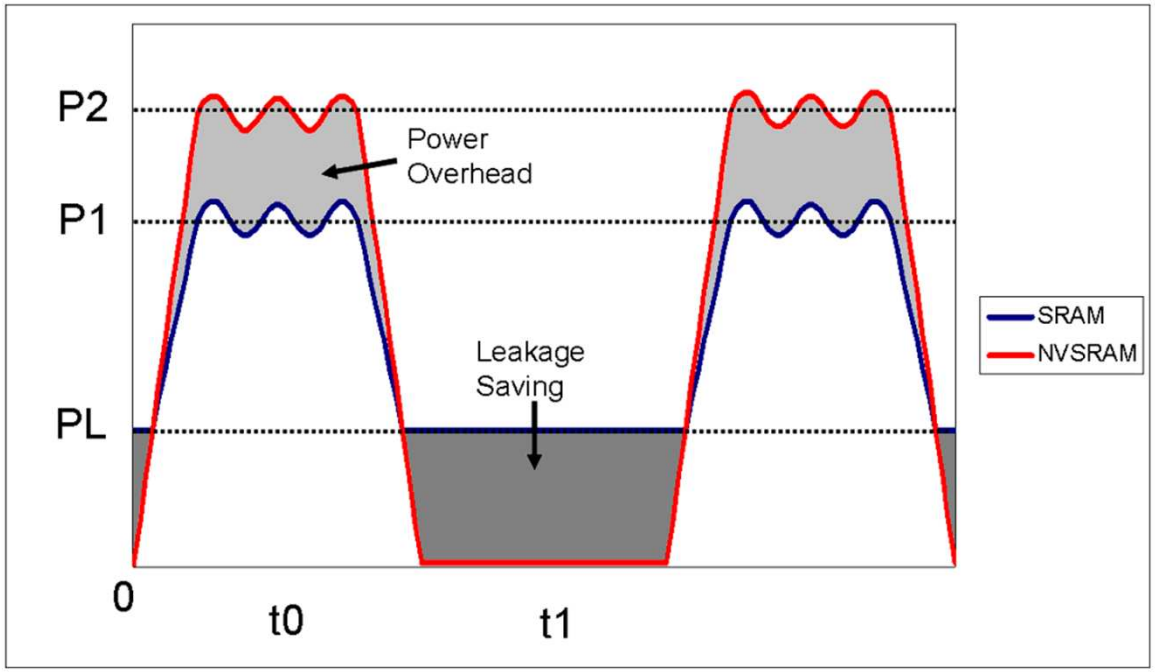
- Main idea:
  - Power-off of FPGA during long idle times
  - Non-Volatile SRAM (ReRAM-based technology) for « instantaneously » restoring FPGA state after power-off

- Questions:
  - Cost of power-off versus ideal idle state (no dynamic power)?
  - Cost of power-on?
  - Is it really « instantaneous »?

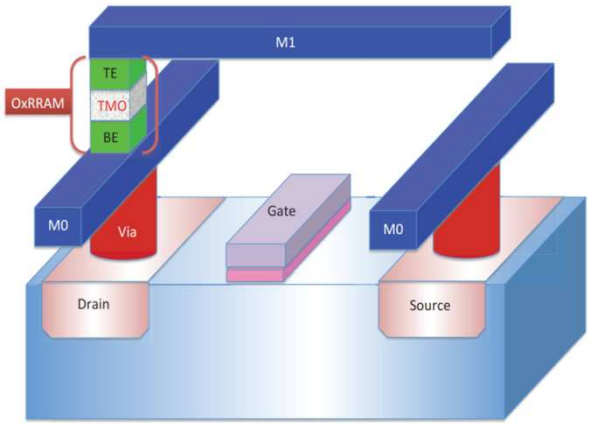
Power gain: Break-Even Time (BET)

- BET = t1/t0 ratio for equivalent power consumption
- Expected gains for higher t1/t0 ratio must be also considered

$$BET = \frac{t_0}{t_0 + t_1} = \frac{1}{1 + \left(\frac{P_2 - P_1}{P_L} \right)}$$

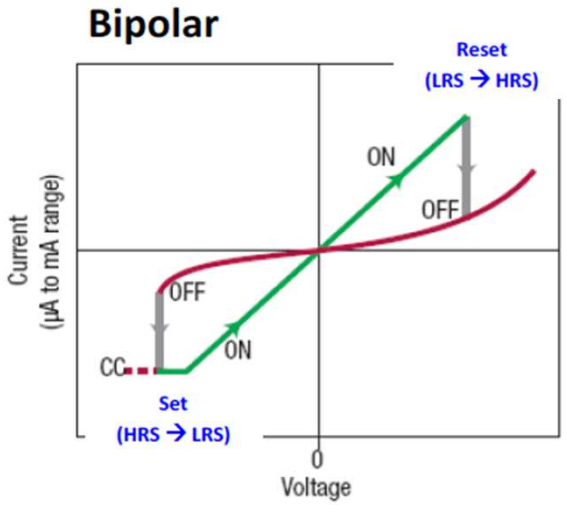


Bipolar Oxide-based Resistive RAM



Features:

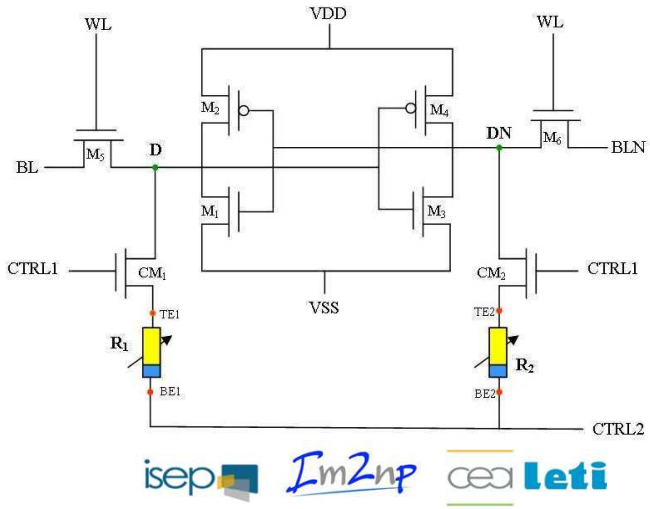
- Non Volatile: data is retained when powered-off
- High density & faster.
- Compatible with CMOS BEOL.



- Exhibits bipolar behavior i.e. Set & Reset at opposite polarities.
- Two stable resistance states LRS (Low Resistance State) and HRS (High Resistance State)
- Resistance ratio (R_{off}/R_{on}) ranging from 10-100

NVSRAM as a configuration point

- 22nm FDSOI LETI technology
  - Low-leakage technology (equiv. 45nm)
- Bipolar OxRRAM compact model from IM2NP
- NVSRAM design from ISEP
- Spice simulation



	Number of min. size transistors
SRAM	11.5
NVSRAM	15.25

NVSRAM operations power costs

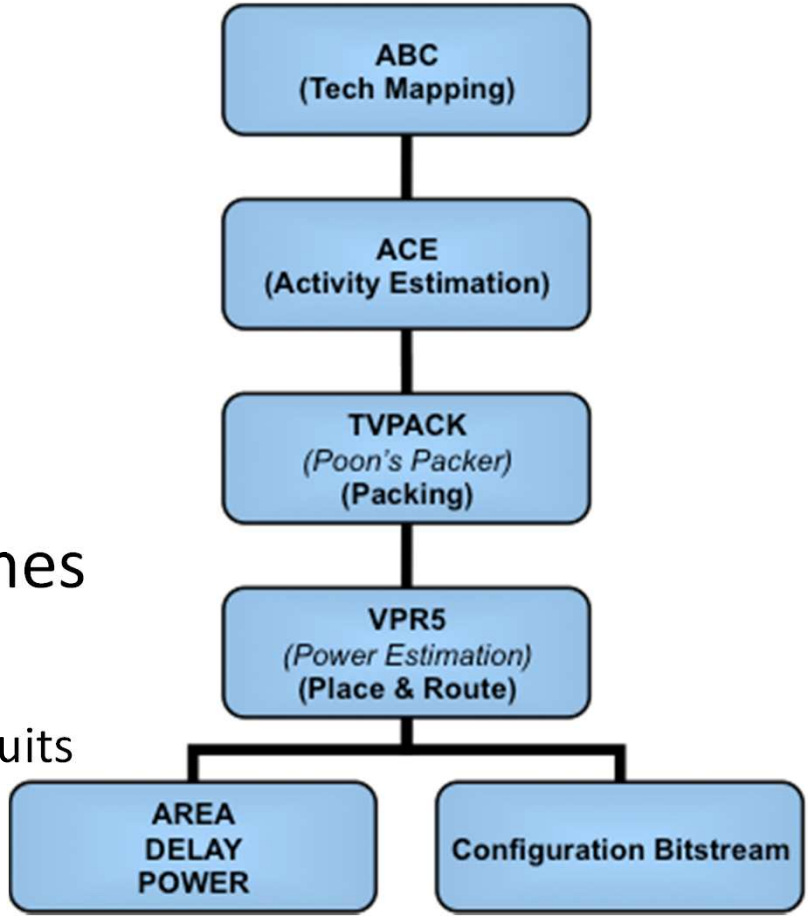
	Pavg(nW)	Duration(ns)	Energy(fJ)
Reset	425	20	8,5
Store	434	20	8,7
Power down	0,06	3800	0,23
Restore	28	**20**	0,56
Avg. power for one switch off-to-on cycle(nW)			**0,20**

=> Instaneous = 20 ns, compatible with most of the applications

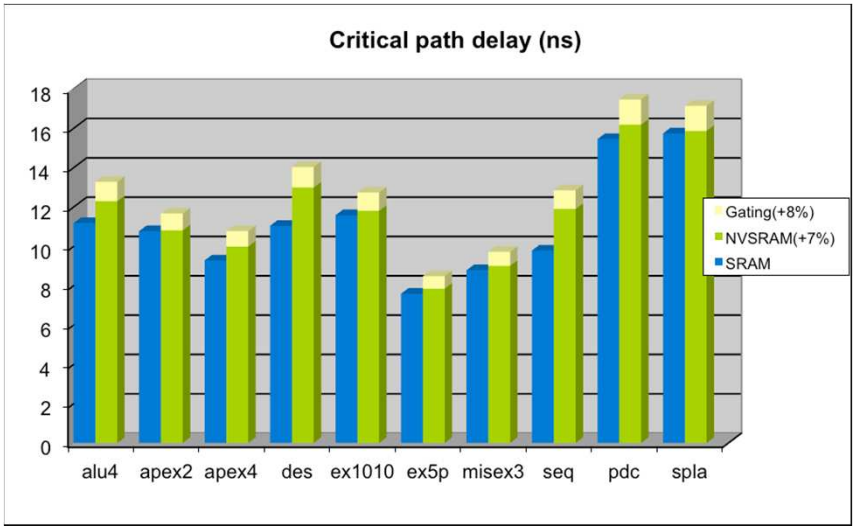
FPGA experimental methodology

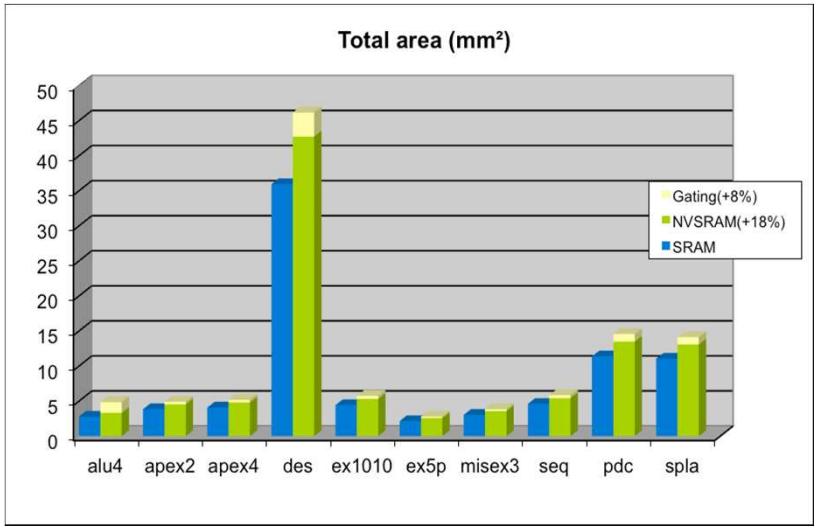
- VPR5 from Toronto
- Added power estimation
- FPGA
  - 10 BLE / CLB
  - 22 Inputs / CLB
- SRAM based design
- NVSRAM with power switches
- Testbenches
  - Combinational and sequential circuits
  - Low to Medium complexity

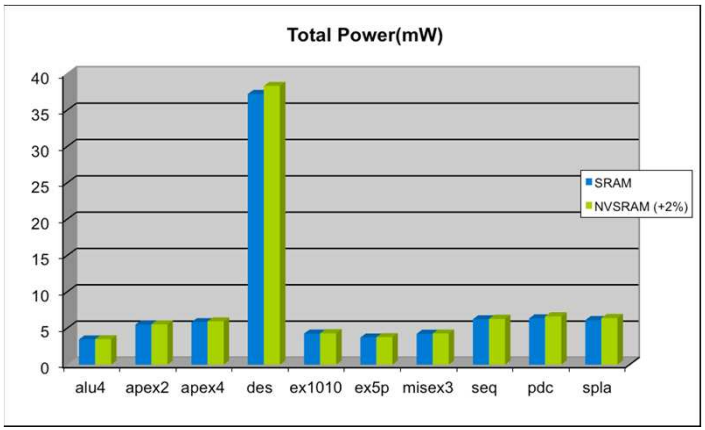
  => ALU4 to cyphering (DES)



Comparison with SRAM-based FPGA





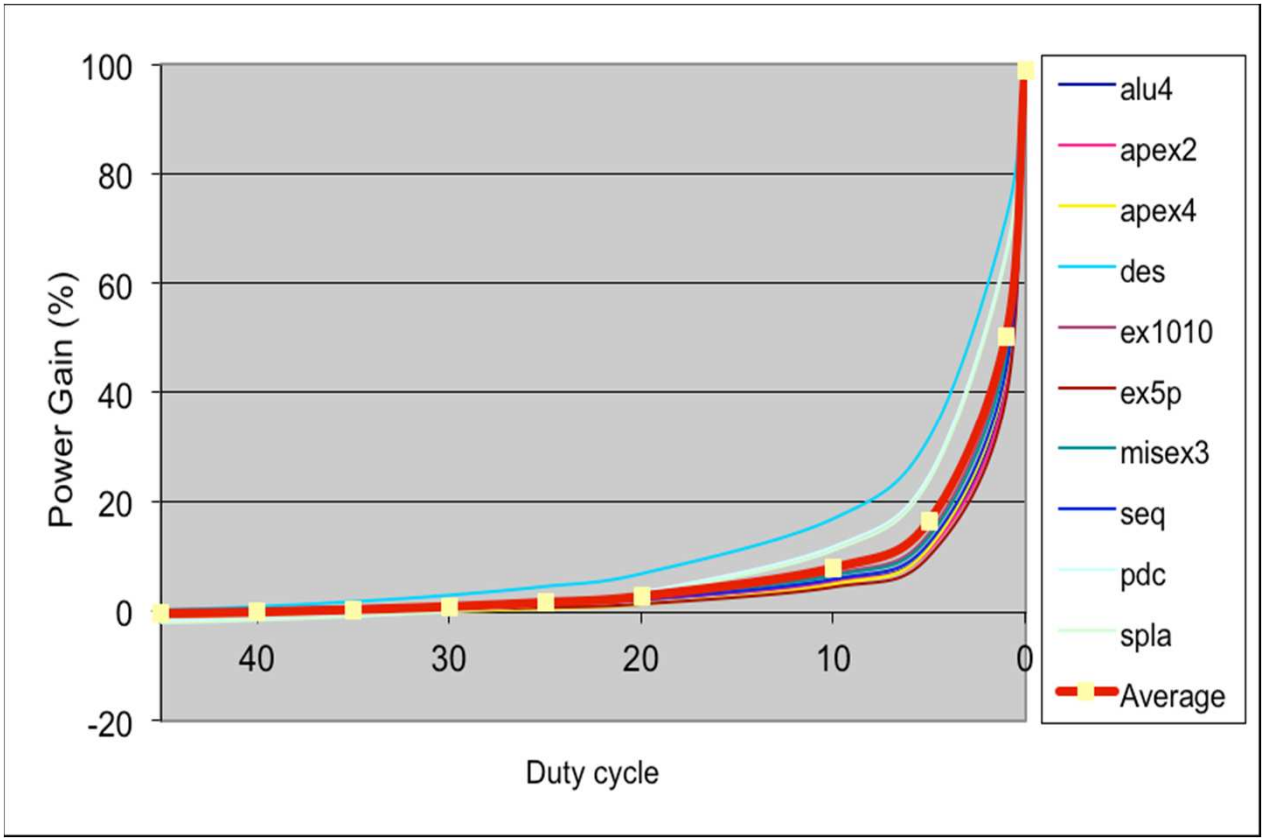


Break-Even Time

Circuit	POH (mW)	PL(µW)	BET (%)
alu4	0,03	24,97	48,24
apex2	0,04	37,90	**50,64**
apex4	0,11	46,66	30,46
des	1,12	994,48	47,01
ex1010	0,04	39,89	47,08
ex5p	0,04	24,63	36,17
misex3	0,04	37,12	46,66
seq	0,05	50,22	48,06
pdc	0,28	129,26	31,36
spla	0,29	120,07	**29,62**
Average			**42,26**

Gains depending on On/Off duty cycle

1% on/off => > 50% power consumption gain



Conclusion & perspectives

- Demonstrated ReRAM-based design for reducing power in FPGA
- Open new application fields for reconfigurable logic
- Efficient cooperation network for speeding-up research to industry
- Perspectives:
  - NVFF for full context « freeze »
  - Applications to other architectures

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- **LETI: Ogun Turkyilmaz, Marina Reyboz, Santhosh Onkaraiah**

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