

Experimental investigation and empirical modeling of the set and reset kinetics of Ag-GeS₂ Conductive Bridging Memories

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Altis Semiconductor

Basic concept of Conductive Bridge Memory

Conducting paths between the device's two terminals in a reversible process that changes electrical resistance by order of magnitudes

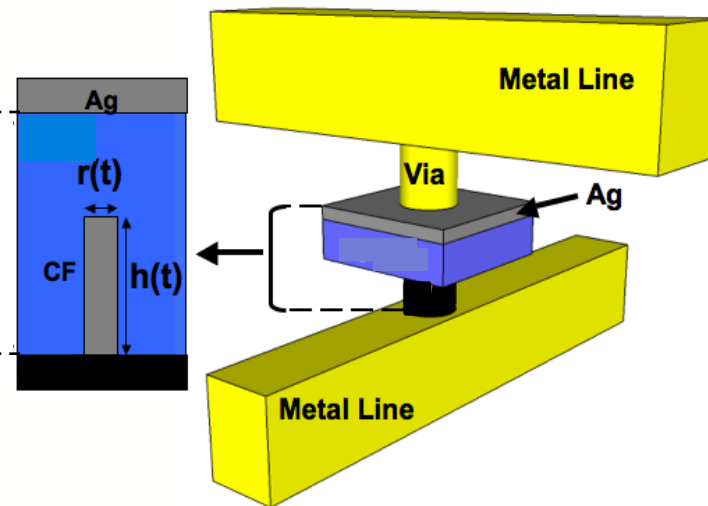
- electrochemical growth and dissolution of metallic filament
- small applied voltage levels and energy
- large non-volatile resistance changes
- simple, high scalable structure

active electrode (**Ag**, Cu)

solid electrolyte:

- Chalcogenides (**Ge_xS_y**, Ge_xSe_y, GeTe, GST, ...)
- high-k (HfO₂, Al₂O₃, Ta₂O₅, ...)

inert electrode (**W**, TiN, Pt, ...)



CBRAM LETI Workplan

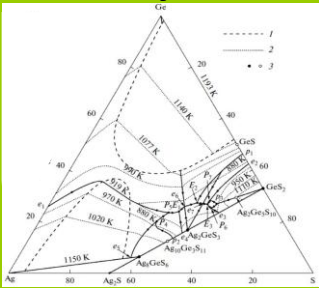
Material research and characterization

Device integration

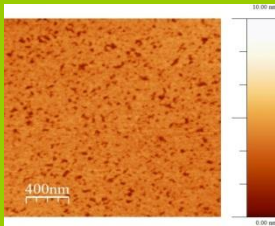
Electrical characterization

Modeling and simulations

New materials, new alloys



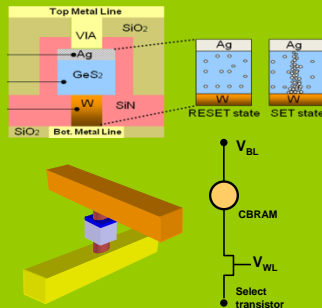
Physico-chemical characterizations



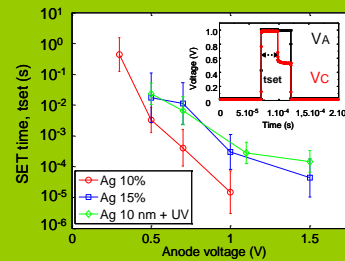
PVD & CVD deposition tools



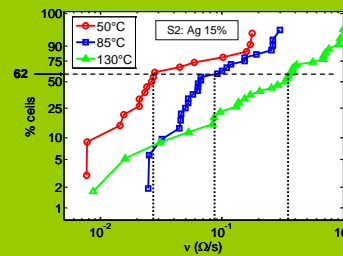
Integration flows



Memory performances...



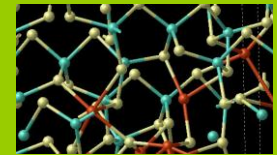
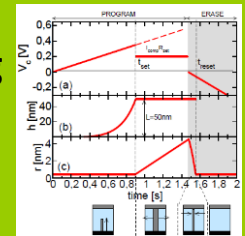
... Specific characterization techniques



Physical understanding

Physical modelling

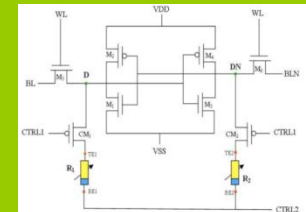
Ab initio calculations



Compact modeling



Design



Outline

- Introduction
- Device physics and modeling
- Operations
- Compact 'non-volatile' logic
- Conclusions

Reaction environment

SET PROCESS

Anodic dissolution

electrochemical electron transfer (Butler-Volmer)
no overpotential, fast reaction
→ not taken into account in the model

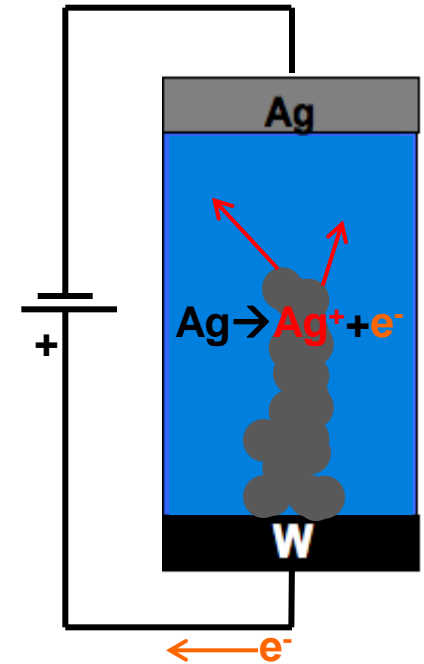
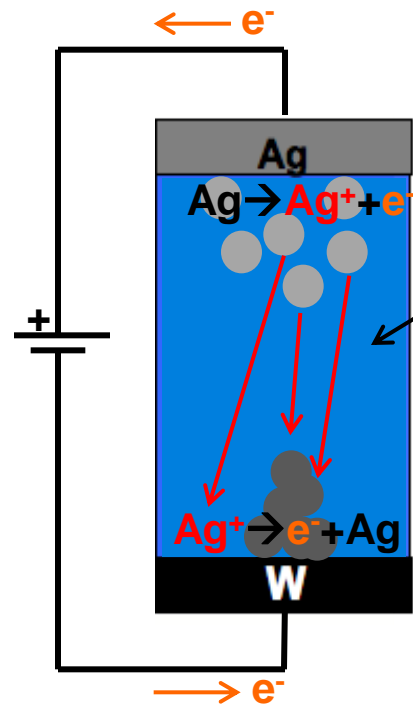
Ionic current

field driven migration process
→ model: Mott Gurney ionic hopping current

Cathodic deposition

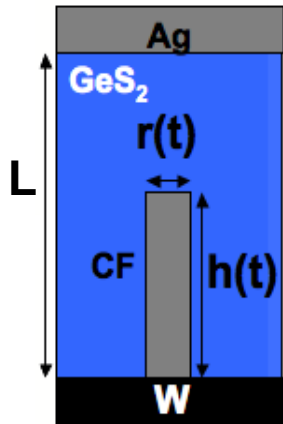
electrochemical electron transfer (Butler-Volmer)
crystallization overpotential
→ taken into account by an empirical parameter (Δ)

RESET PROCESS



Model description

- cylindrical conductive filament: radius $r(t)$; height $h(t)$
- CF vertical and lateral time evolution are assumed to be proportional to the ion current density (Mott Gurney ionic hopping current)



$$\frac{dh}{dt} = \frac{J_h(t)}{qN_i} = v_h \exp\left(\frac{-E_A}{k_B T}\right) \sinh\left(\alpha q \frac{V_c(t) - \Delta}{k_B T}\right)$$

$$\frac{dr}{dt} = \frac{J_r(t)}{qN_i} = v_r \exp\left(\frac{-E_A}{k_B T}\right) \sinh\left(\beta q \frac{V_c(t) - \Delta}{k_B T}\right)$$

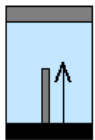
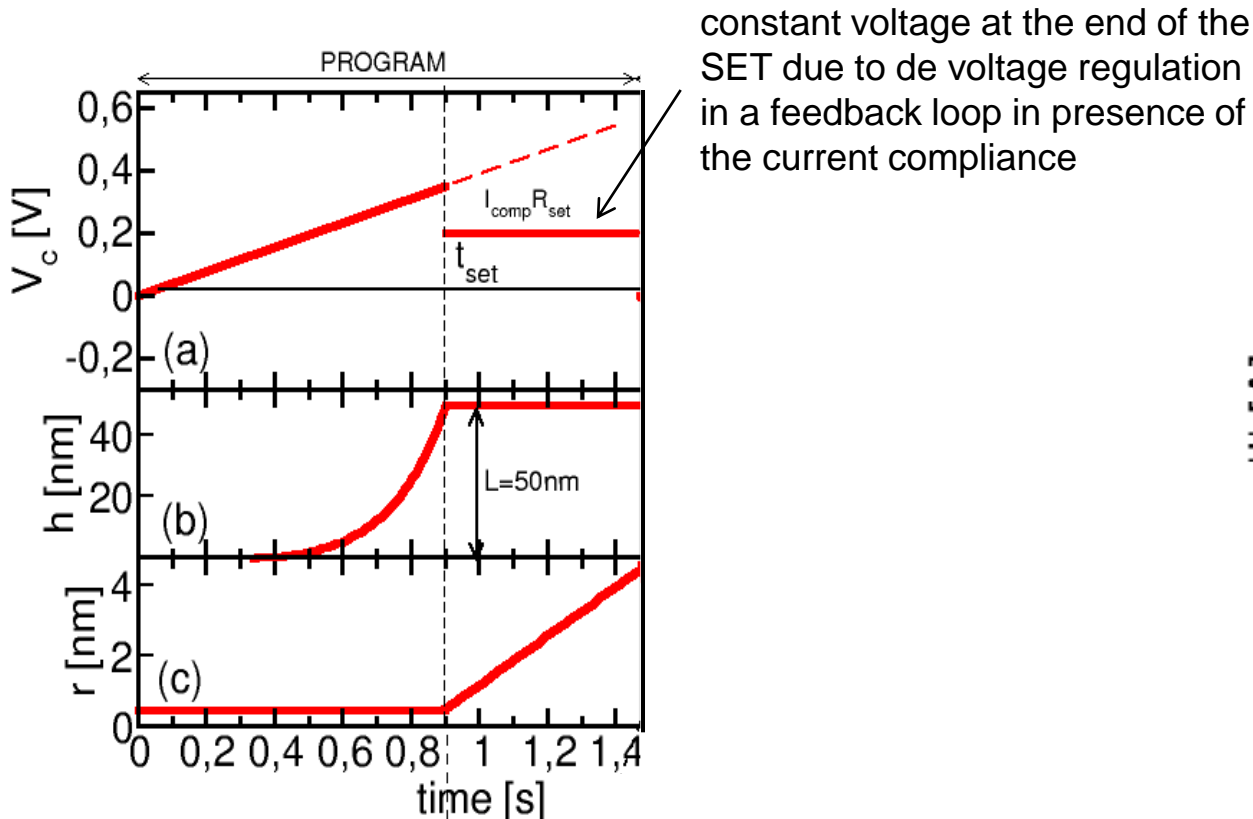
thermally activated & field driven

empirical parameter linked to the overpotential that controls the cathodic reaction

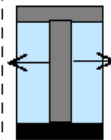
cell resistance:
sum of two series resistors

$$R_c = \frac{\rho_{\text{on}} h(t) + \rho_{\text{off}} (L - h(t))}{\pi r^2(t)}$$

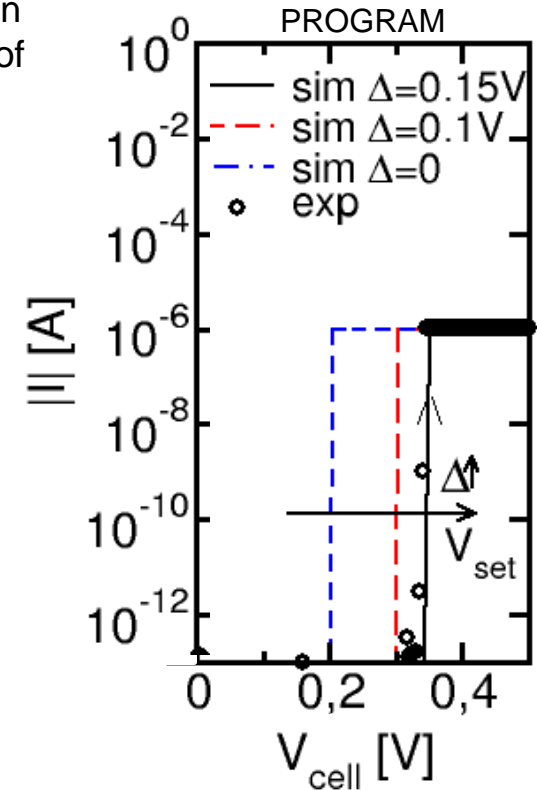
Quasi static program and erase transients



1. vertical growth

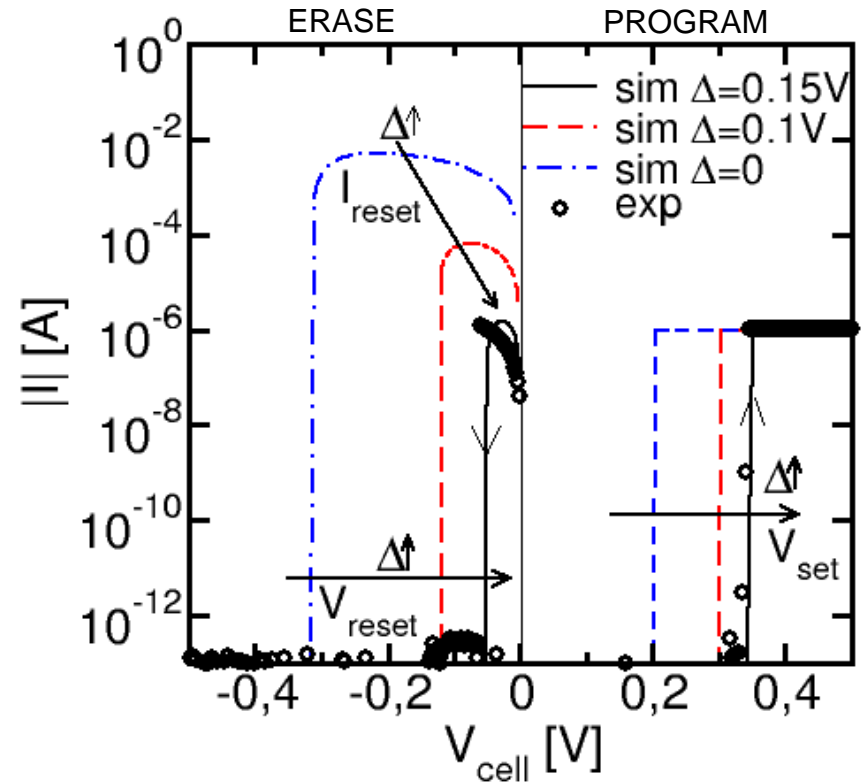
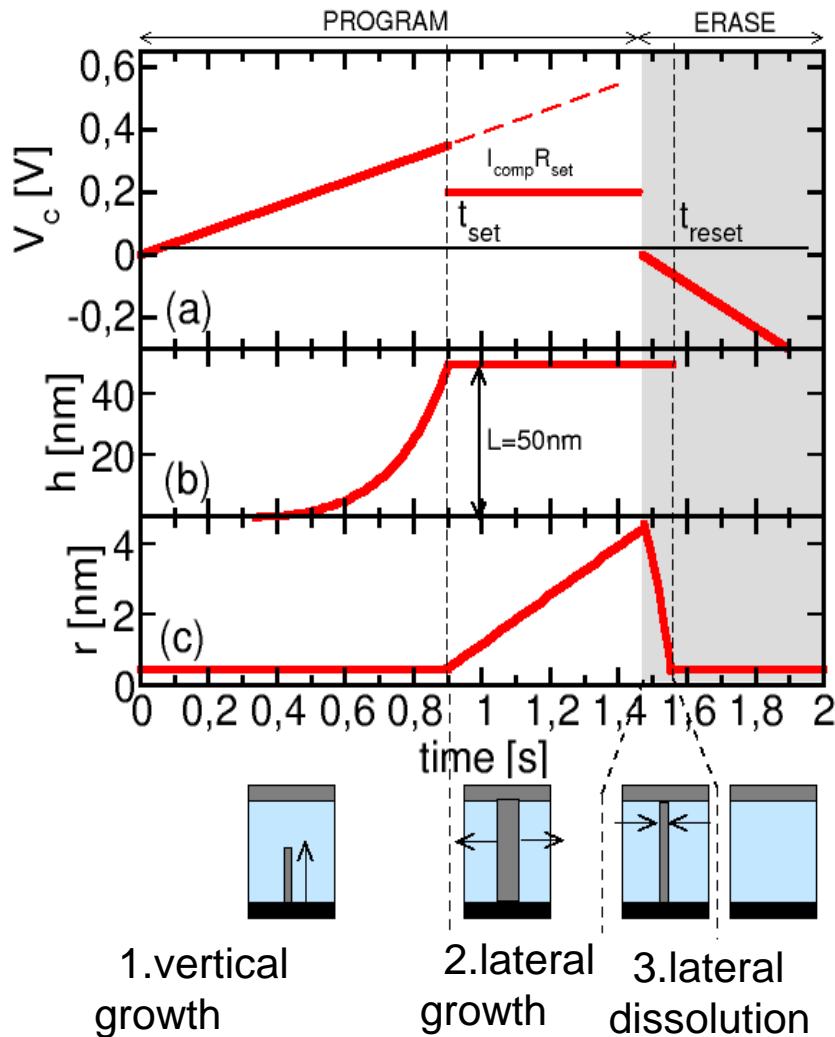


2. lateral growth



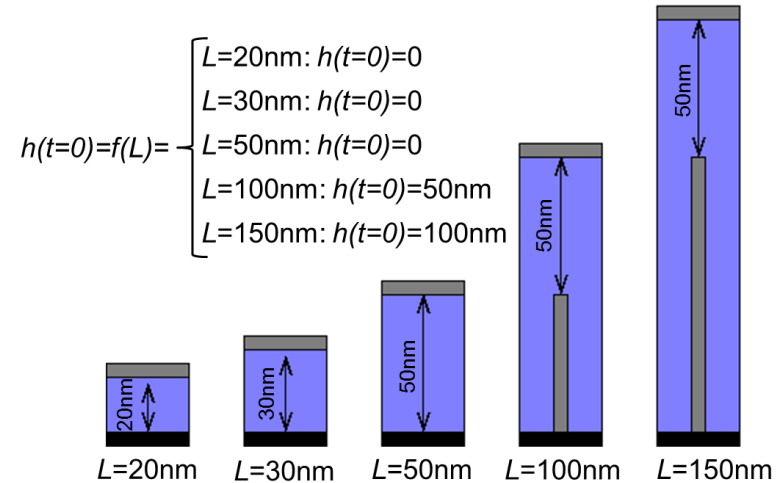
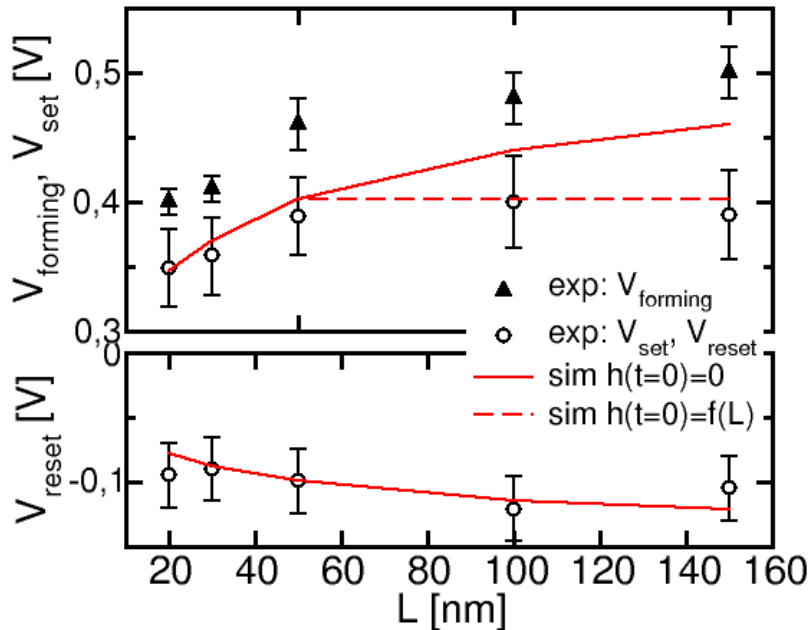
G. Palma et al., « Experimental investigation and empirical modeling of the set and reset kinetics of Ag-GeS₂ Conductive Bridging Memories », IMW 2012

Quasi static program and erase transients



G. Palma et al., « Experimental investigation and empirical modeling of the set and reset kinetics of Ag-GeS₂ Conductive Bridging Memories », IMW 2012

Effect of the active layer thickness

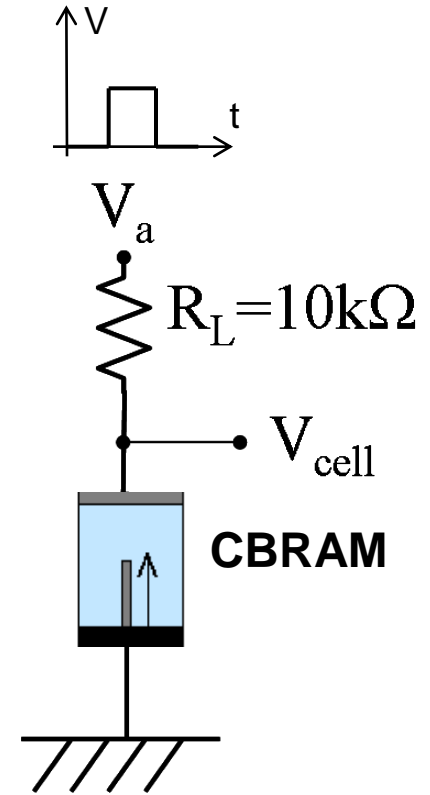
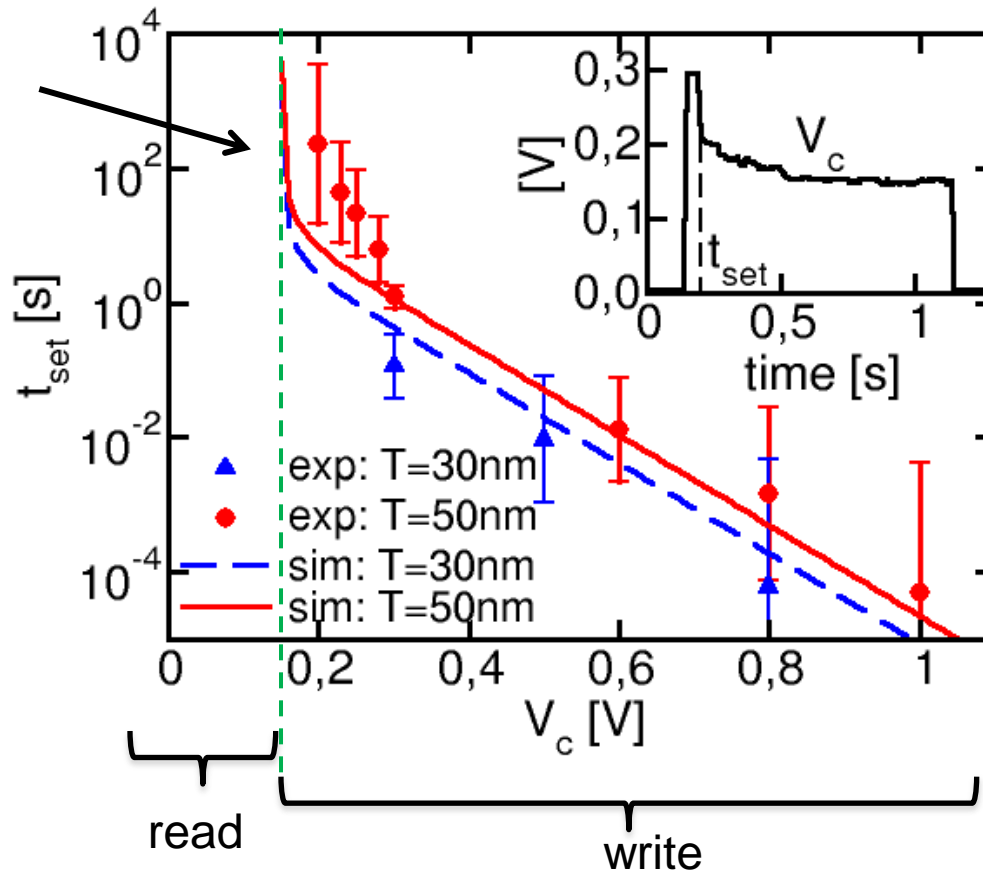


G. Palma et al., « Effect of the active layer thickness and temperature on the switching kinetics of GeS₂-based Conductive Bridge Memories », submitted to SSDM 2012

- **$L < 50$ nm**: the CF in the OFF state is almost completely dissolved \rightarrow increasing L , V_{set} increases
- **$L > 50$ nm**: a portion of the filament might subsist on the W electrode ($h(t=0) \neq 0$) acting as a cathode \rightarrow V_{set} almost independent of L

Programming in pulsed mode

Saturation at low voltage (nucleation overpotential $\Delta=0,15\text{V}$)

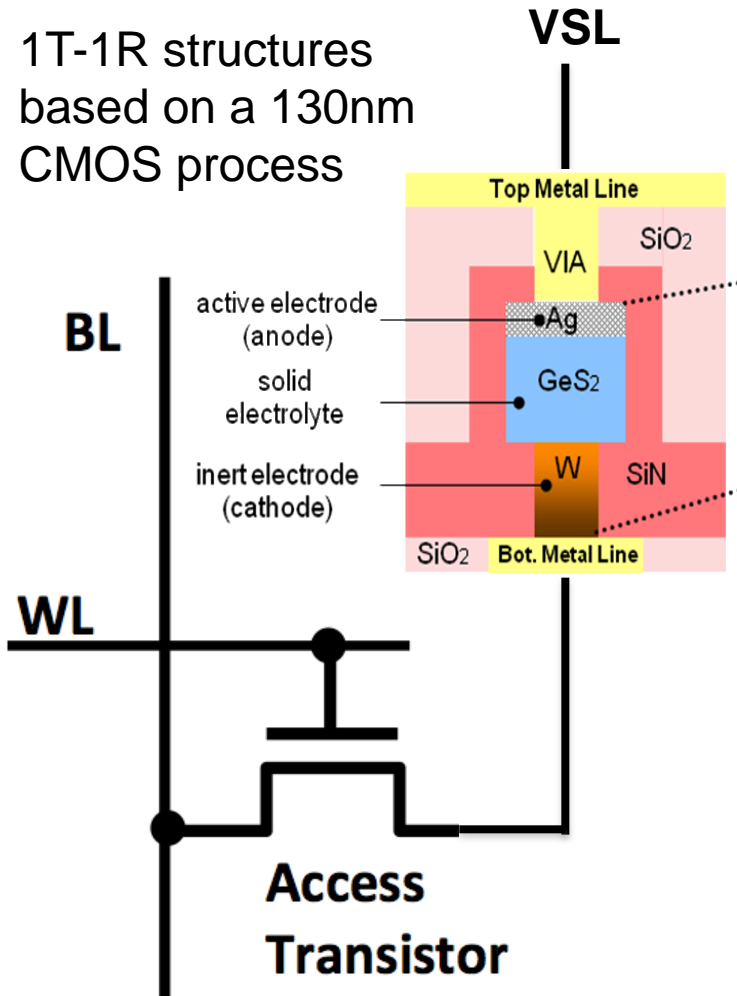


Outline

- Introduction
- Device physics and modeling
- **Operations**
- Compact 'non-volatile' logic
- Conclusions

Studied samples

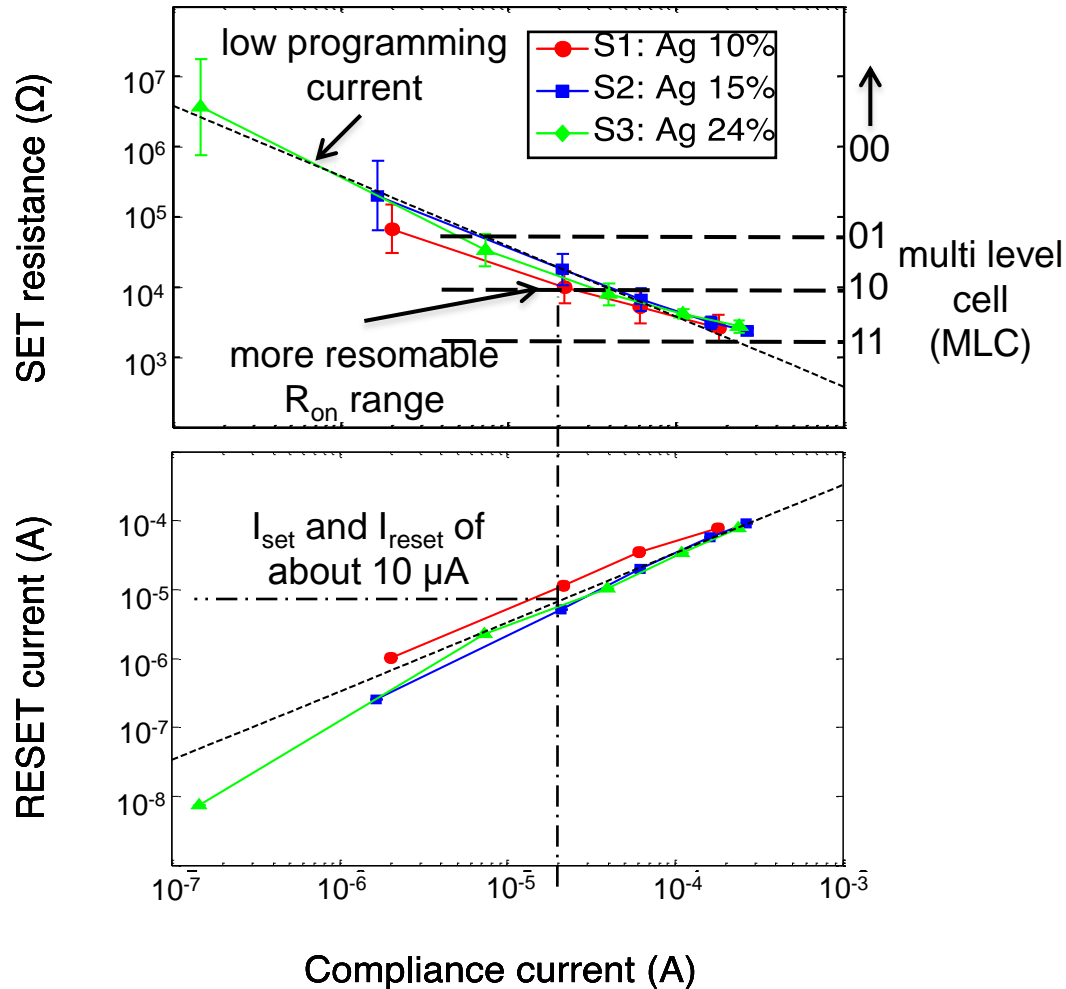
1T-1R structures
based on a 130nm
CMOS process



Sample	<i>%at Ag in the GeS₂ layer (RBS)</i>
S1	10.7
S2	15.2
S3	24

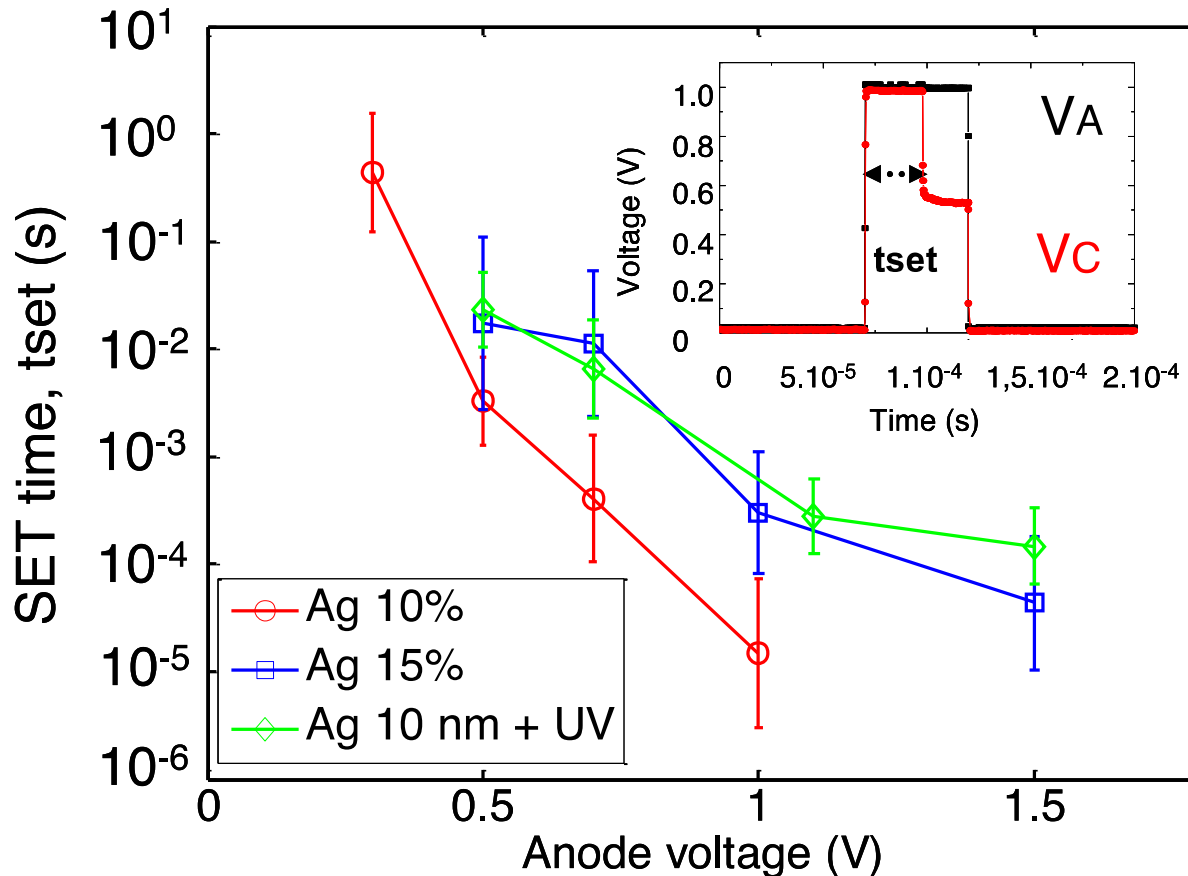
RBS measurements show a constant Ge/S ratio of 0.64-0.66 with different Ag concentrations

On state resistance vs SET/RESET current



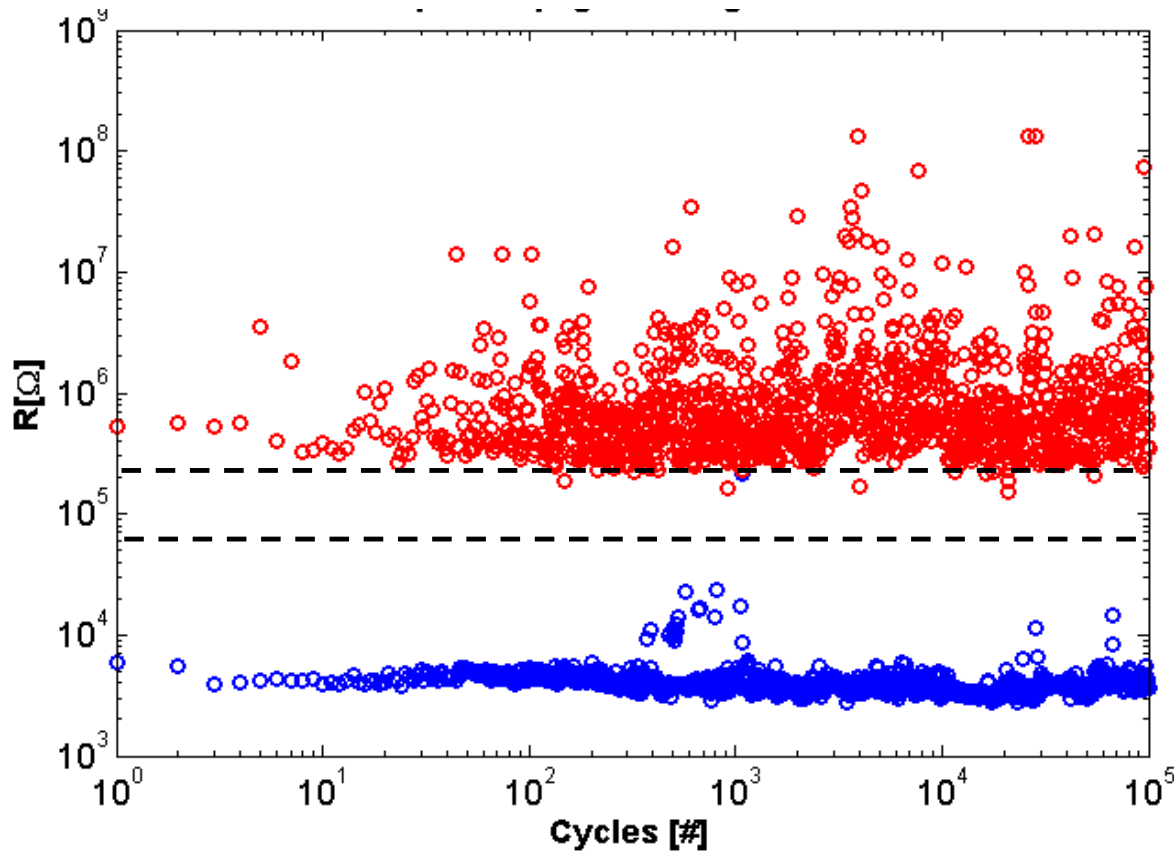
- the SET resistance decreases and the RESET current increases while increasing the SET compliance current
- the SET resistances and the RESET currents are almost completely independent of the Ag doping concentration

Program operation in pulsed mode



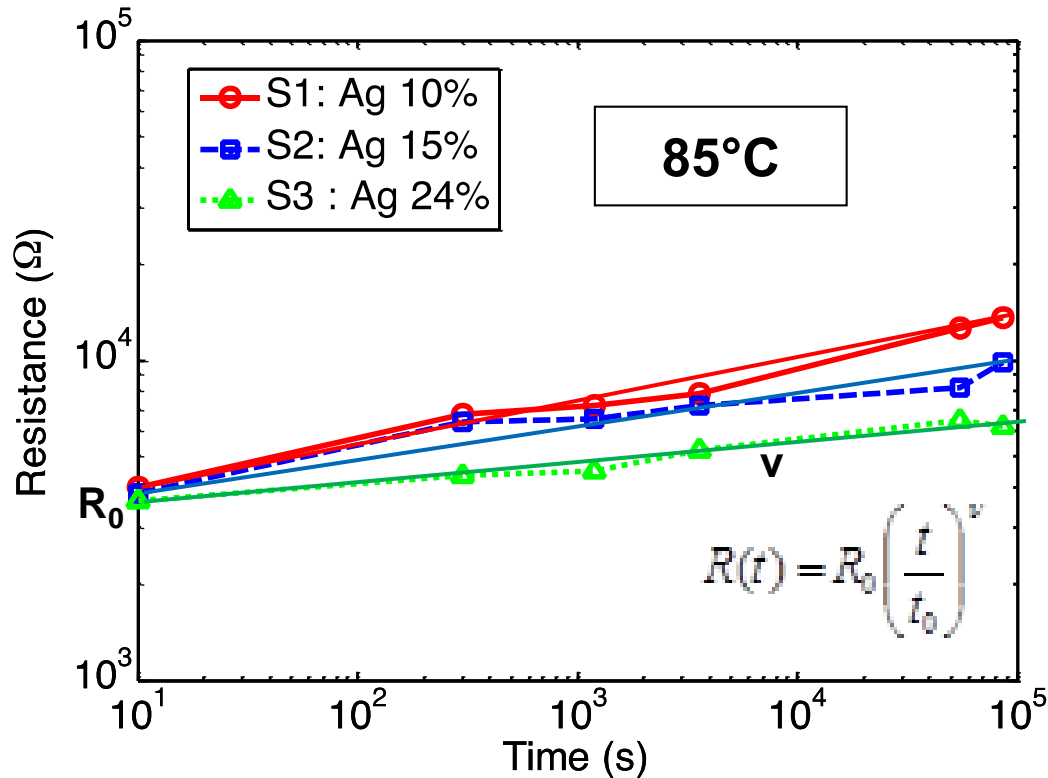
- the SET time increases slightly with the Ag concentration
- **Compliance current in the order of $10\mu\text{A}$ gives programming energy in the orders of nJ !!**

Endurance



**Endurance 10^5
cycles with no
degradation evident
for 15% Ag doped
GeS₂ device (S2)
($I_{\text{comp}} = 10 \mu\text{A}$)**

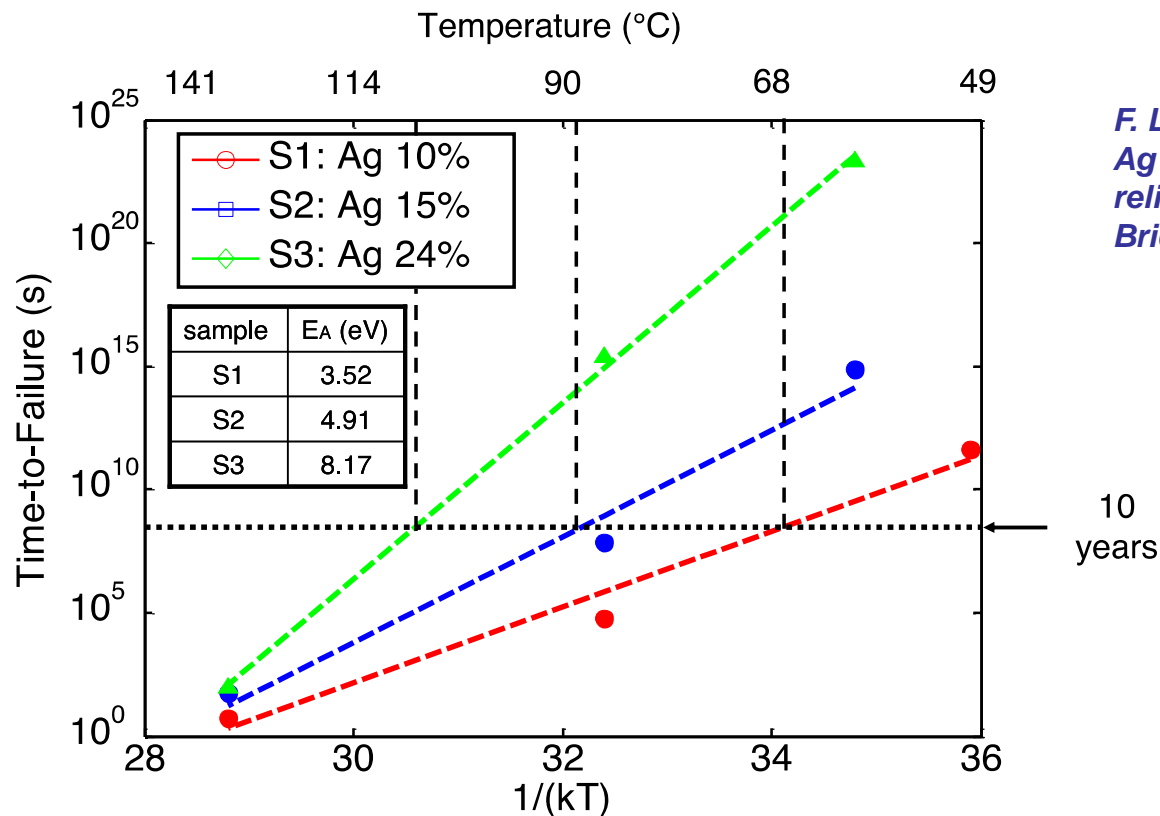
Retention



resistance evolution
averaged on 30 cells

- slower resistance evolution for the highly Ag doped sample
- the resistance-time curves obey a power law \rightarrow we can extrapolate a time-to-failure

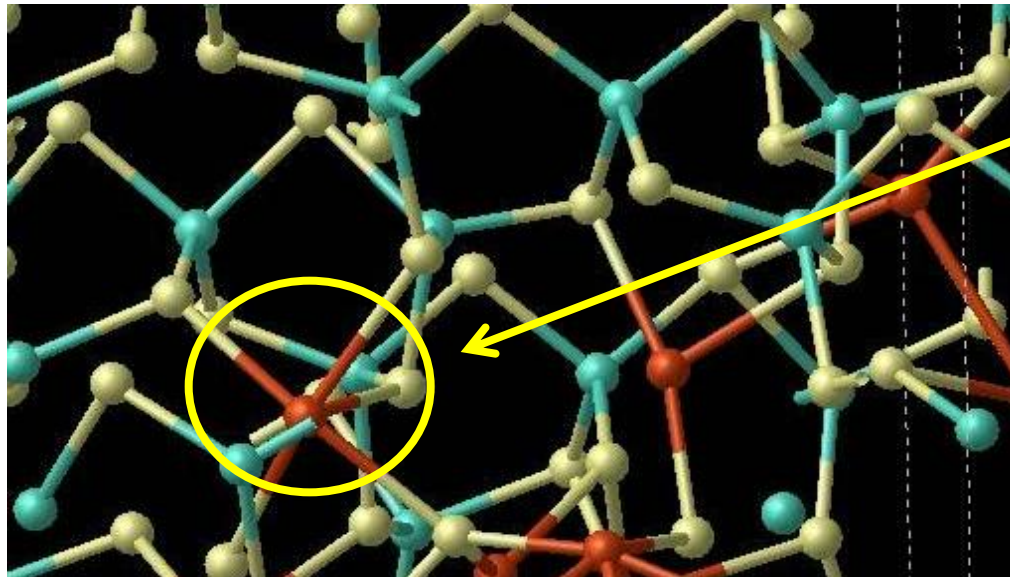
Arrhenius plot of the time-to-failure



F. Longnos et al., « On the impact of Ag doping on performance and reliability of GeS₂-based Conductive Bridge Memories », ESSDERC 2012

- time-to-failure time defined by 10x increase in resistance
- 15%Ag doped GeS₂ extrapolated fail temperature @ 10 years ~ 100 °C

Ag-doped GeS₂ structure



Ag₂S compound

DFT, 200 atoms system
(Red=Ag, green=Ge,
yellow=S)

Ag is always chemically bonded: S atoms react with the Ag thus generating Ag₂S compounds → deficient of Ge-S bonds and unbonded S atoms, hindering the dissolution of additional Ag into the GeS₂

The **Ag diffusion seems to obey the Fick's law** → increasing the Ag doping, the GeS₂ matrix becomes saturated thus limiting the Ag diffusion during the memory operations

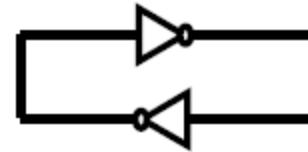
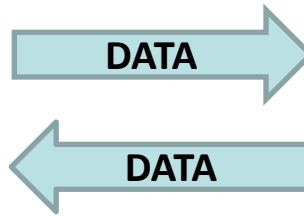
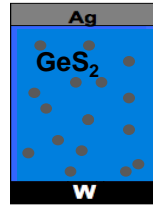
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Study of hybrid “logic-NVM circuits”

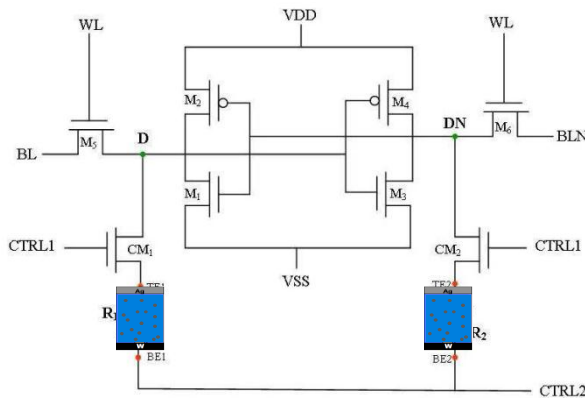
- ERD ITRS 2009: « Nanodevices that implement both logic and memory in the same device would revolutionize circuit and nanoarchitecture implementation »

NV memory
power OFF

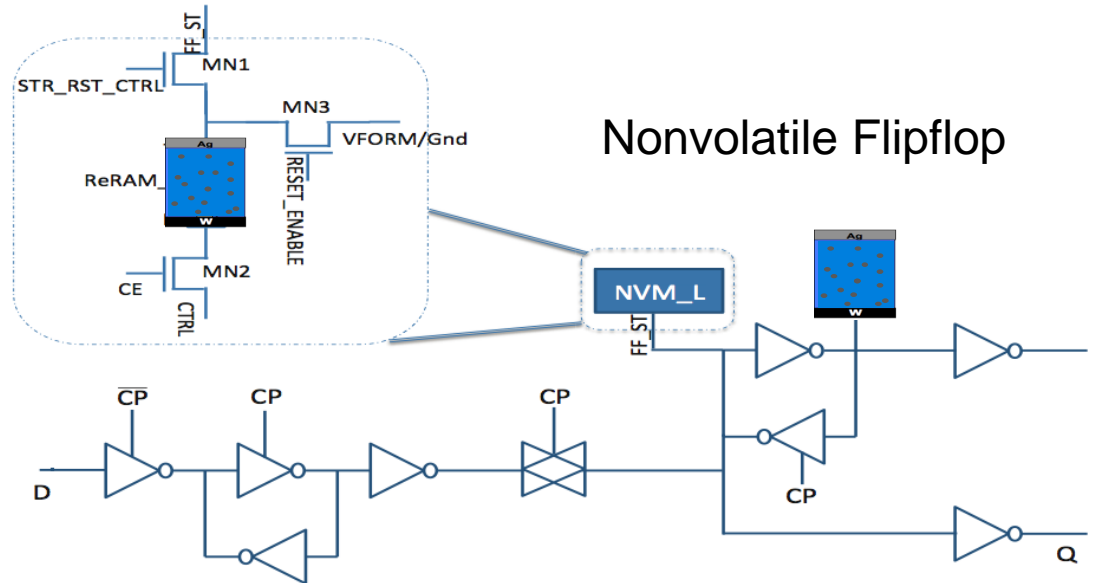


latch
power ON

Nonvolatile-SRAM



Hraziia et al., « Bipolar OxRRAM-based non-volatile 8T2R SRAM for information back-up », EuroSOI 2012



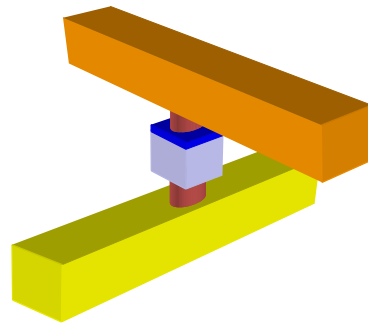
S. Onkaraiah et al., « Bipolar ReRAM Based Non-Volatile Flip-Flops for Low-Power Architectures », NEWCAS 2012

Conclusions and perspectives

- An empirical model able to well reproduce the set and reset kinetics in Ag/GeS₂ CBRAM cells has been developed
 - CBRAM compact model suitable for design implementation
 - design of hybrid Non volatile circuits
- Impact of Ag doping on GeS₂-based CBRAM performance
 - Ag doping leads to a saturated GeS₂ matrix thus limiting the Ag diffusion during the memory data-retention. Other paths of improvements to further to increase operating temperature are under investigation.

Conclusions and perspectives

- RRAM has excellent basic cell properties but scaling, reproducibility/uniformity, reliability, and mass-production issues should be cleared for commercialization



New materials to address soldering issue

- Chalcogenide optimization
 - GeS₂ doping (Sb, Ag, SiO₂...)
- Oxide based electrolytes
 - High-k (Al₂O₃, HfO₂)
 - Electrodes (Cu, ...)



New architectures to study the cell scaling

- Electron beam scaled structures
- μ -trench structures

14th

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Merci de votre attention

