Study of ReRAM based on TiN/ Ta<sub>x</sub>O<sub>y</sub>/TiN integrated into a 65nm advanced CMOS technology

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State of Art – Motivation

General concern

- Increasing demands for embedded memory size for memory access bandwidth
- Market requires low power consumption for SoC used in mobile application

Key Requirements of an Alternative NVM

✓ Low Cost structure
✓ Scalability
✓ Low power
✓ Reliability
Promising results showed on ReRAM in the literature

Panasonic:
Bilayer-TaO based ReRAM using Platinum as electrodes
256Kbit CMOS 180nm, 10^9 cycles, 10 years at 85°C

Z. Wei et al, IEDM 2008

Samsung:
Bilayer-TaO based ReRAM using Platinum as electrodes
Proposed physical model for TaO based on Schottky barrier modulation

M-J. Lee et al., Nature Mat., 2011
• Aim of the work: Demonstrate a TaO Based ReRAM which is:

• **LOW COST NVM SOLUTION!**
  • All materials are cost effective and perfectly compatible with back-end process CMOS
  • ReRAM structure based on mature process based on standard MIM
  • ReRAM integration just with two additional masks

• Extendable to very advanced CMOS technology (Sub 28nm)

• Endurant for application like MTP (multiple time programmable)

• Reliable

• Thermally stable
• State of the art and motivation

• Integration and functioning principle

• TaO properties impact on programming energies

• Mechanism of the switch / how to control the switch

• Switching speed, endurance and reliability

• Thermal behaviors

• Conclusion
Integrated memory structures

ReRAM MIM, Fully CMOS 65nm compatible:

✓ Mature process integration
  ✓ PEALD using TBTDET and Ar/O₂ → TaO
  ✓ PVD → TiN
✓ MIM area down to 1μm²
I-V characteristics: Bipolar switching

Critical parameters
1. Forming (ON) operation:
   - soft breakdown, creation of the critical conductive path
   - Should be compatible with select transistor characteristics
2. 1st reset (OFF) current

TIN/10nm-Ta₂O₅/TiN
Study of forming voltage

- High forming voltage: device function on the weakness zone of MOS transistor
- TaOx leakage current higher than Ta$_2$O$_5$ on
- Hence, Optimum Device: TiN/5nm-Ta$_2$O$_5$/TiN
Conduction mechanism before Forming

Poole Frenkel modeling equations

\[
\begin{align*}
(1) \quad \ln(J/E) & = A \frac{\beta_{PF}}{k_BT} \sqrt{E} + B \Rightarrow \ln\left(\frac{J}{E}\right) \rightarrow f(\sqrt{V*C}) \\
(2) \quad \ln(J) & = A \frac{\beta_{PF}}{k_B} \frac{1}{T} + B \Rightarrow \ln(J) \rightarrow f\left(\frac{1}{T}\right)
\end{align*}
\]

Straight lines behavior indicate Poole–Frenkel conduction mechanism
Study of the Reset current

✓ Lowest 1st reset in thin dielectric

✓ TaOx shows a low reading window even if its reset current is lower than Ta2O5 reset current

=> Thereafter, studies will be focused only on results of TiN/5nm-Ta2O5/TiN device
Outline

• State of the art and motivation
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Device area impact and possible mechanisms

Local filament conduction path suggested
✓ No issue for shrinkability
Controlling the filament formation

Filament formation (ON state) could be controlled through current compliance in view of low power operation.

Hypothesis:
- The filament diameter increases with ON current compliance.

✓ The resistance of the reset state can be controlled by the compliance current of the Set state.
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Switching speed and Repeatability

- Set operation can be realized at pulse time faster than 10ns
- ON operations are performed with very low voltage (~ 0.5V)

- SET/RESET operations repeatability up to 100 pulsed cycles
- Acceptable read margin (ROFF/RON ~100)

- Promising for MTP applications

Example of cycling on Ta2O5 with a serial resistor of 1K pulsed operated (set: V=2.5V, tp=10µs, Reset: V=-1.2V, tp=50µs)
Retention at high temperature

Retention behavior of TiN/Ta$_2$O$_5$/TiN device under 250°C with constant read voltage of 0.1V

- Cells store data after a bake of 250°C during 24 hours
- Cells are fully functional after the bake at 250°C during 24 hours
Thermal stability: ON/OFF dependence with temperature

Temperature dependence of ON/OFF resistance of TiN/Ta₂O₅/TiN device (vread=0.1V)

ON/OFF cycling dependence to temperature. Resistance values (left coordinate axis) and Voltages values (right coordinate axis)

No significant impact of temperature on ON / OFF Resistance =>
Good thermal stability of 5nm - thick Ta₂O₅ temperature up to 125°C
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Conclusions

- **Forming and Reset operations have a close relationship with the TaO properties and thicknesses**

- **Evidence of the filamentary conduction on TaO. Good shrinkability suggested**

- **ON/OFF operations demonstrated with very low voltage (0.5V) and high speed (10ns)**

- **Reliable devices (ON/OFF retention during 24h at 250°C)**

- **Thermal stability (a key issue for SoC applications) is successfully demonstrated up to 125°C**

TiN/Ta$_{2-x}$O$_{5-y}$/TiN structures are very promising for future MTP applications beyond 28 nm node technology.
Thank you!

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Figure 5. Forming/cycling results for a RRAM stack with thin layer of AlOx added next to the same HfOx used for figures 3, 4. No reset is observed for current compliances of 10µA, 100µA, and 1mA.